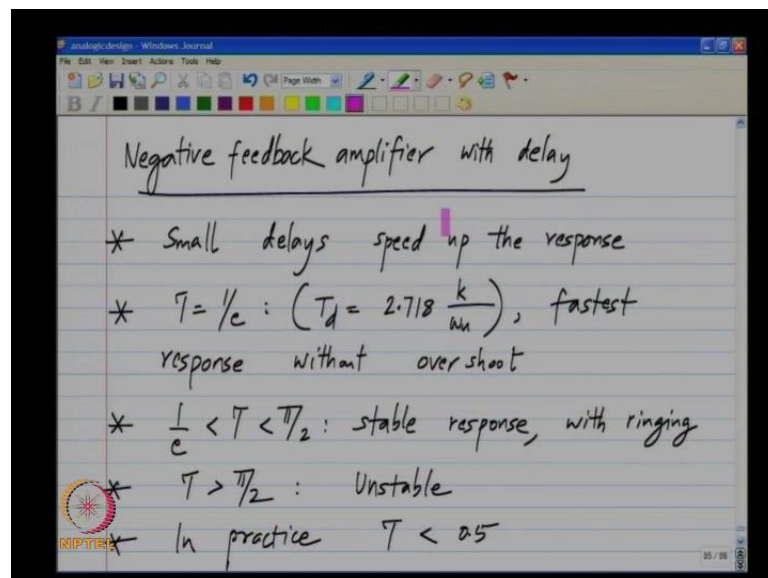


Analog Integrated Circuit Design
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 8
Negative Feedback Amplifier with Parasitic Poles and Zeros

Hello and welcome to the eighth lecture of analog integrated circuit design. At the end of the previous class we summarized what happens in negative feedback amplifier with delay will just go through again at quickly.

(Refer Slide Time: 00:24)

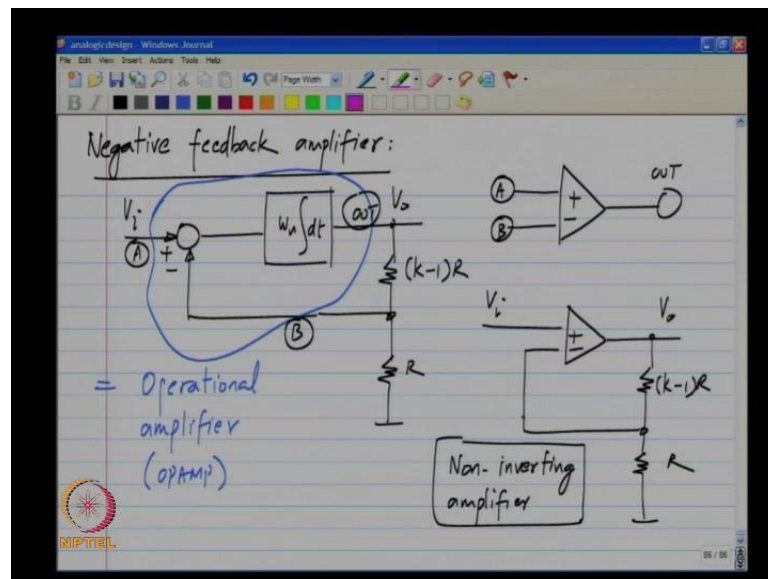


What we saw was that small delays in the negative feedback amplifier actually speed up the response. So, it is beneficial, but this happens for up to tow equal 1 by e approximately 0.36 times the time constant, this should be 1 by 2.718 naught 2.718. Up to this value of the delay, you will actually speed up the response compared to not having any delay and this gives you the fastest response without having an overshoot. And if the delay is between 1 by e and pi by 2 that is one by e times the time constant and pi by 2 times the time constant we get a stable response, but with ringing and for tow greater than pi by 2 about one and half time the time constant the responses unstable. That is even without an input you will end up with an output I mean.

And in practice you cannot have a lot of ringing. So, you have to limit the value of tow to under 0.5 that is of the time constant of the system. What will do today is to look at how

a delay comes about in real system because in a real system will not have an ideal delay as we were assuming so far, that was just a model for any delay that may come. A real system what happens is you have parasitic poles and zeros in the frequencies response at different points of the loop. We will see how the equivalent contribute to delay and what to do about it. To do this we have to first look at how we can realize the negative feedback system that we have.

(Refer Slide Time: 02:09)



So, the essential component of the negative feedback system is taking the difference between in input and some feedback quantity, and integrating the difference. And you drive the output in a way that the differences minimize that is the essence of negative feedback. So, every negative feedback system needs to have a way to take some difference and way to integrate the difference. Now, because this is so widely used this taking of the difference and the integration is integrated into a single block, and it is a very familiar block, and this is known as the operational amplifier or opamp for short.

So, essentially an opamp is a block that takes the difference and integrates it were this terminals correspond to this. So, this is what an opamp is, it is a block that takes the difference between 2 quantities and integrates the difference. And you can very easily see that the opamp can be wired up to make the negative feedback amplifier that we have. If I have to use the opamp in this diagram what I will do is ill apply V_i to a the plus terminal of opamp, and the output is divided using the voltage divider, and the

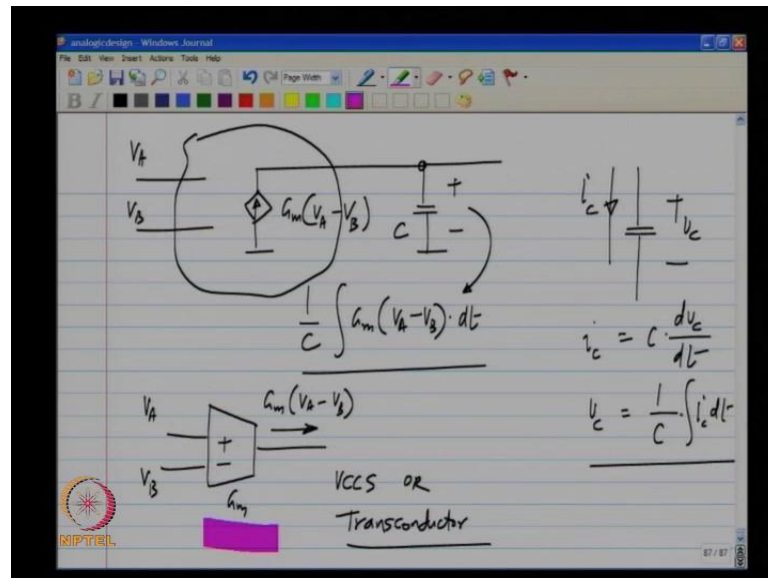
output of the voltage dividers forms the other input to the opamp. The difference between these two is integrated to try V_{naught} and many of you may be familiar with this circuit as the classical non-inverting amplifier. So, we have to realize a block that makes, you have to realize the block that is the difference and then integrates the difference.

Now, if you look at a circuit elements that we have we have resistor capacitor an inductor, and we can also make a variety of control sources using transistor. This you are already familiar with you have a common source amplifier, common gate and common drain. And some of them are useful as voltage control voltage sources and some of them as current control current sources and so on.

And the transistor by itself act as a voltage control current source either the MOS transistor are the bi polar junction transistor act as a voltage control current source. But here what we need is integration that is integration with respect to time. And of the element we know the inductor and capacitor are elements to do integration, the inductor integrates the voltage across it to give you the current through the inductor, the capacitor integrates the current through it to give you the voltage across the capacitor.

Now, inductors are rather bulky and if you try to realize the kind of integrates that you want in an opamp, using inductor it will become very large and there impractical to realize. So, we are left with only one alternative that is use a capacitor to get the function of integration.

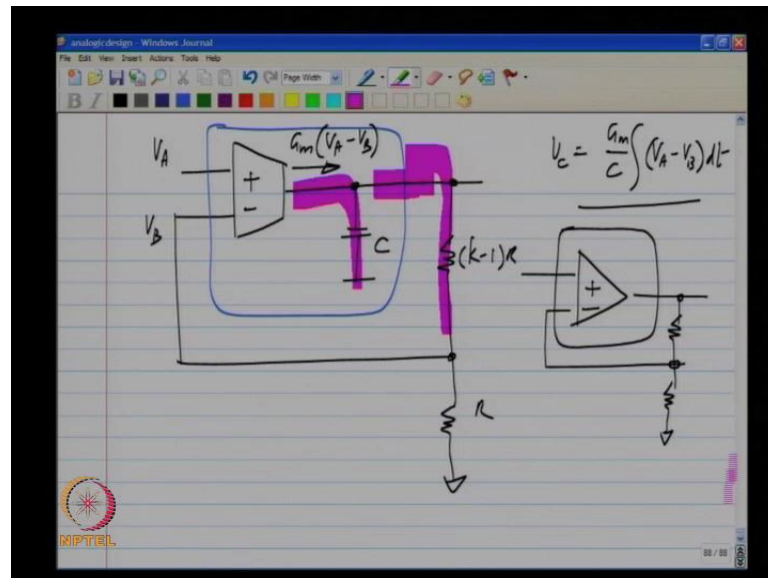
(Refer Slide Time: 06:30)



So, a capacitor which has a voltage V_c across it and connect I_c through it, obey is the relationship I_c is c times the derivative of voltage or V_c is 1 over c integral of the current. Now, the difference is available as a voltage, this is a difference voltage V_e and this is for has to be integrator, but the capacitor integrates the current. So, we first have to convert the difference voltage, I will call this V_A and V_B and I have to integrate the difference between V_A and V_B . So, I first use a voltage control current source which gives a current proportional to V_A minus V_B . And this current flows through a capacitor C to result in a voltage which is 1 over c integral of G_m times V_A minus V_B with respect to time.

Now, this particular block it is a voltage control current source and integrates circuit design a different symbol is use for it, for the same function. We use the symbol that is somewhat similar to that of an opamp and this symbol means a voltage control current source. And you typically write the value of the proportionality constant next to the voltage next to the symbol. And this means that a current G_m times V_A minus V_B will be forced out of this block. So, this is the voltage control current source or a trans-conductor and this value G_m is the trans-conductance of this trans-conductor. Now, I will rewrite my integrator using the symbol.

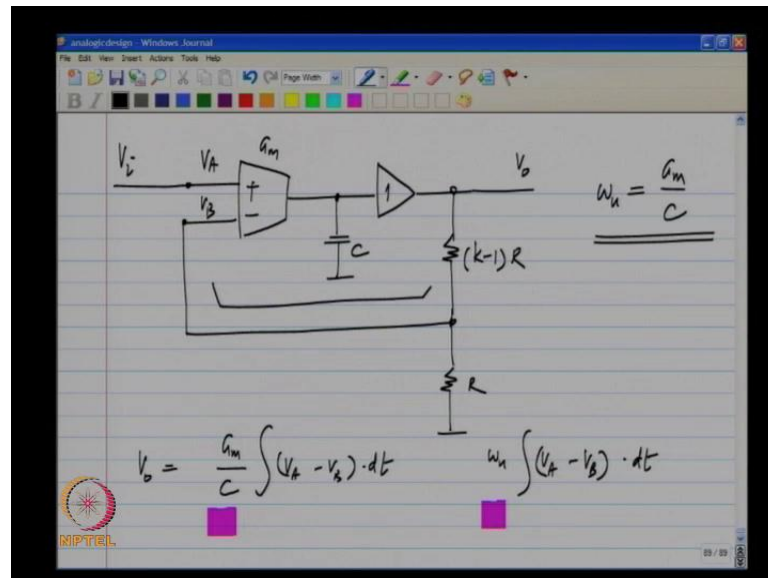
(Refer Slide Time: 09:07)



So, now we know that the voltage at the output are the voltage across the capacitor is some constant times integral of V_A minus V_B with respect to time. Now, we can try using this in our amplifier, earlier we wrote down the picture of the amplifier which is like this where these opamp is realized using this circuit, we can try to do this. So, think about the circuit of a moment and see if it works, we will immediately see a big problem here.

The current G_m times V_A minus V_B was supposed to flow through the capacitor, but the moment you connecting these resistances some of that current will flow through the resistances. And integration function is not exactly what you wanted, to prevent this you have to make sure that no current is drawn from this point and all of the current from the trans-conductor goes into the capacitor and to do that will use a voltage control voltage source are a voltage buffer.

(Refer Slide Time: 11:06)

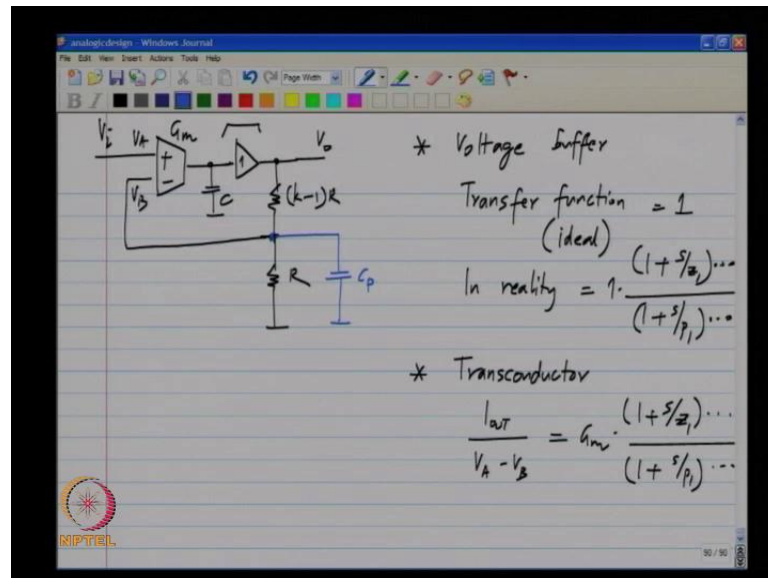


So, finally, the picture of opamp it just follows we have the trans-conductor which drives the output current into a capacitor. And to avoid drawing any further current from this, we use a voltage buffer this means that the voltage here as the same as the voltage there, but the input resistance this block is infinity an output resistant is 0. So, this block does not drawn any current from the capacitor and the same time it can provide any current that is required from its output.

So, this now is the equivalent circuits of the opamp this is way in which opamp can be realized. Usually there is lot more detailed circuitry inside, but for now this will do. If you look at the transfer function of opamp by itself, that is the trans-function this block the output voltage the opamp is given by G_m by C integral V_A minus V_B with respect to time. And what we wanted was for it to be ω_u integral V_A minus V_B with respect to time. If you just match the terms you will immediately see that the unity gain frequency of the integrator ω_u is G_m the value trans-conductor that we use divided by C , the value of integrator capacitor that will use.

So, ω_u is G_m by c . So, this is the exactly equivalent to the amplifier that we had earlier using the integrator and we can do our analyses with this only have to do is to substitute ω_u by it is value which is G_m by c . So, now, what can happen here that can give you delay. So, there are several possibilities.

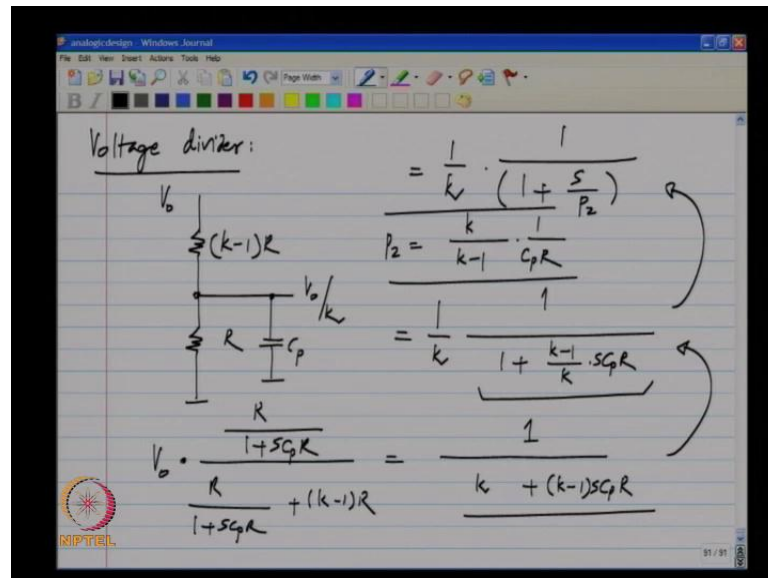
(Refer Slide Time: 13:37)



So, first of all we have the voltage buffer and ideally the transfer function of this, it is one and in reality it could have some poles and zeros, it will be one times 1 plus s by z one and it could have multiple zeros also it could have multiple poles. Now, the exact transfer function depends on the details of the circuit that is used to implement the buffer. Similarly, the trans-conductor the trans-conductor as it is I out by V in were V in refers to the different voltage V A minus V B this is V A and that is V B. So, I out my V A minus V B should be a real number G m, but what can happen is depending on how complicated is circuit you use to realize that trans-conductor this could also have extra poles and zeros.

So, I am just showing the transfer function in a general form there can be extra poles in the trans-conductor, there can be extra poles in the buffer. Also first of all the reason for getting a extra poles any system is that there are parasitic capacitance from every node of the circuit to ground. So, for instance here ideally there is nothing but in reality there will a capacitor. So, let me call that C p with respect to ground C p between that point and ground now what happens because of this let us examine the voltage divided by itself.

(Refer Slide Time: 16:29)



If they have V_{naught} here I will get V_{naught} divided by k , but in reality I have this, in addition to that I have let's say a single parasitic capacitor C_p over there V_{naught} here what comes out here. You can again use the voltage divider formula to get the result, the voltage that comes there is v_{naught} times the impedance of this part of the circuit. And the impedance of this part of circuit is R times 1 by C_p by R plus 1 by $S C_p$ that is a parallel combination R and 1 by $S C_p$ and this is equal to R by 1 plus $S C_p R$.

So, this is a useful result remember that if you have a resistor and a capacitance in parallel the combined impedance is given by this formula R by 1 plus $S C_p$ what it means is that at low frequencies at d c the capacitor an open circuit it does not come into picture. So, at d c that impedance as to be R and that we see is case because we have R divided by 1 plus $S C_p R$ and for d c s zero. So, impedance of this r combination at d c is R and low frequency when the current through capacitor negligible the impedance is still R .

This means that the second term in the denominator is negligible compared to 1 . At very high frequency the capacitor tense to act like a short circuit infects most of the current goes through the capacitor instead of the register. Again if you now imagine that the second term in the denominator here is much more in the first term we will get approximately R by $S C_p R$, R 1 by $S C_p$. So, at high frequencies you is only the capacitor C_p this expression make since.

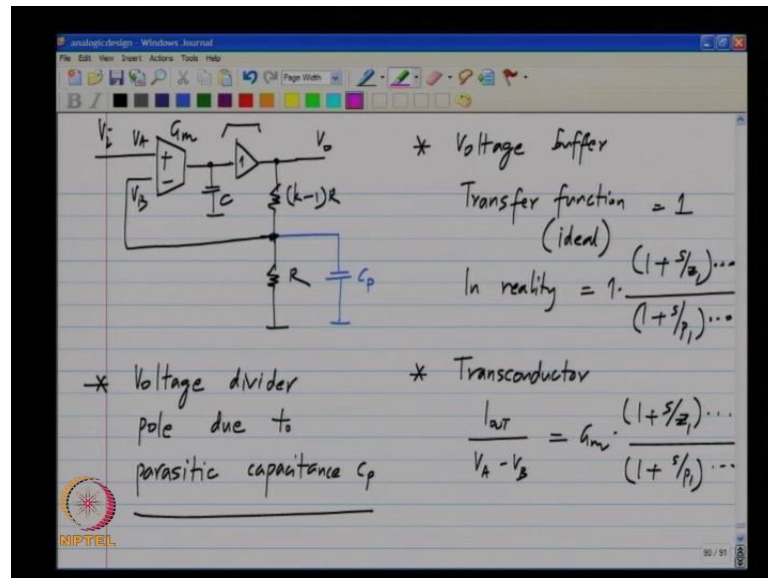
And as I mention introductory lecture whenever you analyze a circuit it is important to interpret the result and make sure that they make introduce sense, what the expression is saying is that at low frequency is the impedance will be R at high frequency is the impedance will be C_p . As you well know when you have a parallel combination, the impedance is dominated by the lowest impedance, at low frequency is the impedance of capacitor very high, it does not come into picture at, but it high frequency is the impedance of capacitor very low. And that is what dominates the picture.

Coming back to the transfer function of the voltage divider I have R by $1 + C_p R$ that is the impedance of lower part divided by R by $1 + S C_p r$ plus k minus 1 times R . Let me erase this part of it and this if I simplify, I will get r divided by k times R plus K minus 1 $S C_p R$ square and R cancels out to give you 1 by k plus k minus 1 times $S C_p$ times R . And this I will rewrite by pulling out 1 by k outside. So, what this is saying is you have 1 by k which is the value would you expect times one divided by some term that contains a pole, some term that contains S .

So, if you look at this, this part of the function is one at d c when S equals 0 . And it keep decreasing as is decreasing as ω increases, at it very high-frequency is what happens is because of this capacitor C_p which act like short circuit, even if you apply a voltage here at a high if the voltage have high frequency component, that component will shorted out the ground and you will see nothing at the output.

So, this is the transfer function voltage divider and I will rewrite this as 1 by k which is ideal value times some transfer function that contains a single pole. I will denote that p_2 in the case p_2 happened to be k minus 1 by k times. So, I would at k by k minus one times 1 by $C_p R$. So, in the voltage divider also you can have a pole and will see soon that I pole acts like a delay.

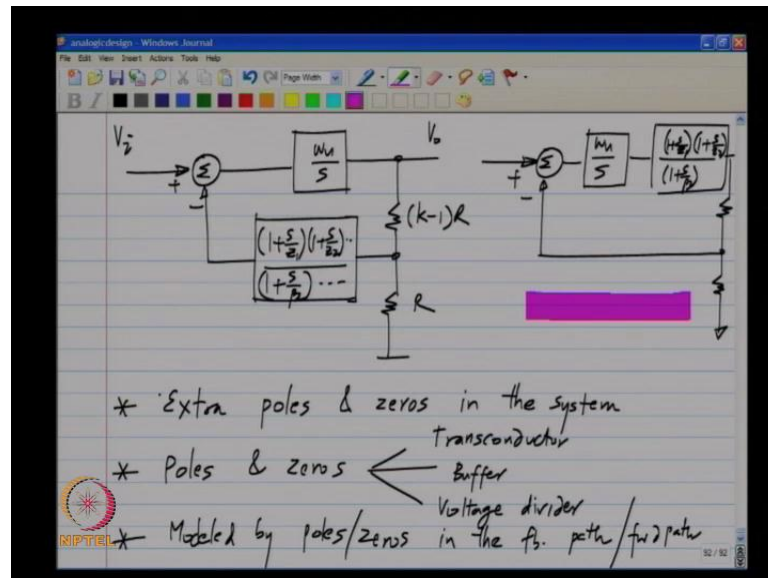
(Refer Slide Time: 22:31)



So, to summarize voltage divider as a pole due to parasitic capacitance C_p . So, every part of the circuit the transconductor the voltage buffer and the voltage dividers can have extra pole and all. So, extra zeros for the voltage dividers only illustrated an extra pole, but it is possible to have a zero, if there is capacitance between this point and that point. So, in general you will not have only the transfer function that you want you will also have extra poles and zeros and that is how delays come into the system, that is how all this non-ideality comes into the system.

Now, why is this equivalent to delay will later do that quantitative analyses and see how the equivalent is produced, but for now just note that if you apply a step to V_{in} and initially the voltage here is zero, what happens is the capacitor holds the voltage at zero it does not rise up behind zero. So, effectively the even though apply input step, the output is not a step for some time it will remain at a zero its slowly increases. So, that is equivalent to delay. Basically the capacitor needs time to charge, it takes some for the voltage across the capacitor to change and that manufactured itself as a delay in the system. So, in general we can have additional poles and zeros in the transfer function that is what it means.

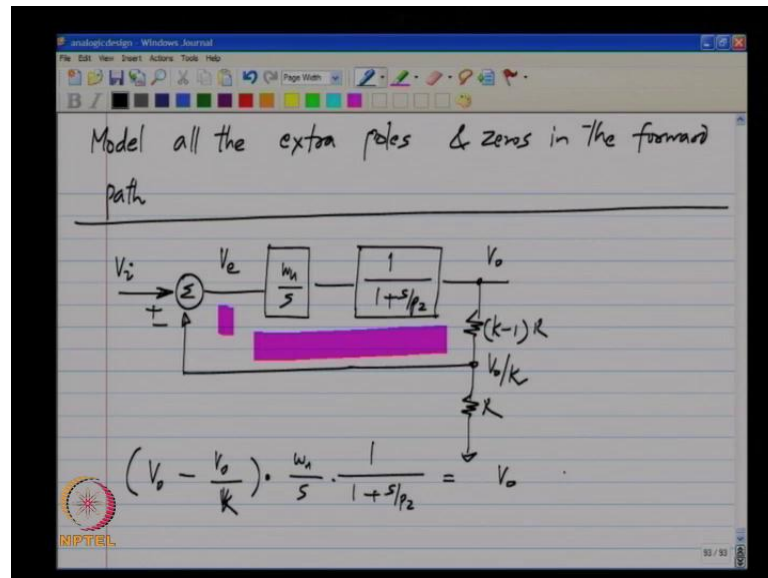
(Refer Slide Time: 24:26)



So, while modeling the delay I will use the Laplace transform here, while modeling the delay what I done was to insert an ideal delay $e^{-s t}$. Now, I have to do is not this ideal delay, but some extra factor that as all kinds of poles and zeros. Now, as I mentioned earlier the poles and zeros come inside the realization of the integrator, and in the divider and so on. But we can club the effect all of that into poles and zeros in the feedback path. So, in general in the feedback path we can have $1 + s/z_1, 1 + s/z_2$ etcetera divided by $1 + s/p_1, 1 + s/p_2$ and similar other factors.

So, the bottom line is that is there are extra poles and zeros in the system, and this poles and zeros can be any part of this system that is that trans conductor, the buffer or even the voltage divider. But for the sake of convenience in analyses we will club all of that into as set up poles and zeros in the feedback path. We can equivalently model the same using extra poles and zeros in the forward path as well, because what we are looking for is the effect of the poles and zeros, in general in general terms and we can do it also in the forward path like that. So, for the sake of convenience I will use this particular model, but you will reach the same conclusion whether you use that one are the other one.

(Refer Slide Time: 27:59)



So, I will model all the extra poles and zeros in the forward path and also I do not want to make my life. So, complicated that I can't you solve the problem. So, first what I will do it i will assume a single extra pole and forward path then we will assume to extra poles and then we will draw conclusion then we have multiple extra poles and zeros in the forward path. I have the integration and let say I have one extra pole.

So, now what I can do is I can calculate V_{naught} by V_i for this case and see what happens, the way to calculate V_{naught} by V_i is like we were doing all along the voltage dividers gives an output V_{naught} by k and I have to take the difference V_i minus V_{naught} by k . So, that is the voltage here and clearly V_e times the transfer function of this whole thing equals V_{naught} and this voltage times ω_n by s 1 by 1 plus s by p_2 equals v_{naught} .

(Refer Slide Time: 30:02)

The image shows a digital journal window with the following handwritten equations:

$$\left(V_i - \frac{V_o}{k} \right) \frac{\omega_u}{s} \frac{1}{1 + \frac{s}{p_2}} = V_o$$

$$V_i = V_o \cdot \frac{s}{\omega_u} \cdot \left(1 + \frac{s}{p_2} \right) + \frac{V_o}{k}$$

$$\frac{V_o}{V_i} = \frac{1}{\frac{1}{k} + \frac{s}{\omega_u} + \frac{s^2}{\omega_u p_2}}$$

$$= k \frac{1}{1 + \frac{s \cdot k}{\omega_u} + \frac{s^2 \cdot k}{\omega_u p_2}}$$

And I just re-write this as I get this by moving this part to the right-hand side I also take this part and move it to the right-hand side. So, v naught by V i transfer to be one by one over k plus s by ω_u plus s square by $\omega_u p_2$, which can be rewritten by pulling k outside s square k by ω_u time p_2 .

So, I removed k outside because the that is ideal again of the amplifier and we see that the d c picture is not affected by the addition of the pole and this is what you expect you expect that poles give you delay and something happens to high frequencies, but as for d c is concerned the d c gain of this block is unity. So, nothing happens at d c that is different from what was happening before the d c gain of this path is still infinite. And finally, you will get a d c gain for overall system that is equal to k that you can see here if you substitute s equal to 0, you will get this function to be equal to k .

(Refer Slide Time: 32:06)

The image shows a digital journal with handwritten mathematical derivations. At the top, the transfer function is given as $\frac{V_o}{V_i} = k \frac{1}{1 + s \cdot \frac{k}{\omega_n} + s^2 \frac{k}{\omega_n^2}}$. This is then rewritten in standard form as $= k \cdot \left[\frac{\omega_n^2/k}{s^2 + s \cdot \zeta + \frac{\omega_n^2}{k}} \right] \frac{\zeta}{2 \sqrt{\frac{\omega_n^2}{k}}}$. Below this, the natural frequency is defined as $\omega_n = \sqrt{\frac{\omega_n^2}{k}}$ and the damping factor is defined as $\zeta = \frac{1}{2} \frac{\sqrt{\zeta}}{\sqrt{\omega_n/k}}$. A small logo for 'NIPTEL' is visible in the bottom left corner of the journal page.

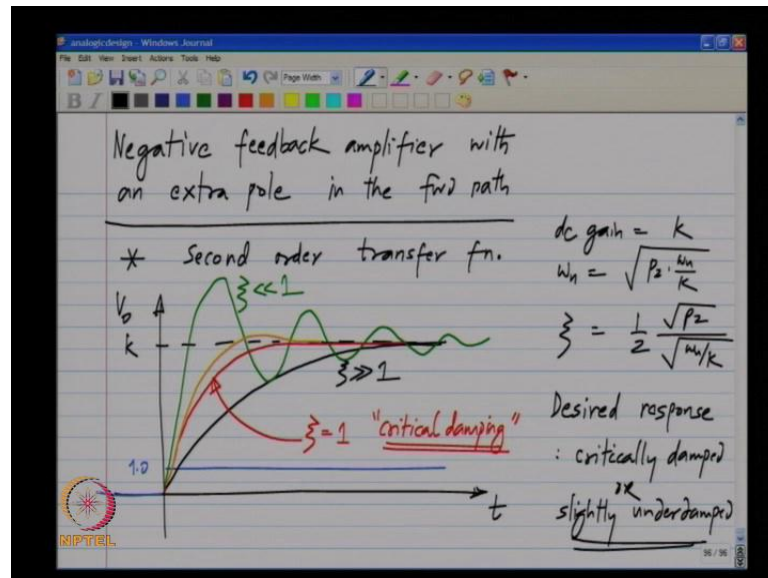
So, rewriting this again V_o by V_i is ideal gain k times 1 plus 1 by 1 plus s times k by ω_n plus s square times k by ω_n times ω_n^2 . Which I will rewrite in the standard form for a second order systems by multiplying both the numerator and denominator by ω_n^2 by k . The reason to write it, like this is that you are already familiar with second-order systems, we analyzed spring mass system and the LC system and know a lot of about it. So, we will reduce it to a similar form that you familiar and then see how the system behaves.

Now, the second-order system is characterize by its natural frequency and the damping factor. Natural frequency is usually denoted by ω_n and the damping factor is ζ , and for the this values the denominator should be a squares plus $2 \zeta \omega_n$ times s plus ω_n^2 . If the denominator this form this is ω_n^2 and the coefficient of s^2 $\zeta \omega_n$, the coefficient of a square is 1 . Now, by matching the term between denominator that we have and the denominator here we can find out the value of ω_n and the damping factor ζ .

So, ω_n comes out to be square root of ω_n^2 divided by k and ζ terms out to be ζ divided by 2 divided by ω_n , which is ω_n^2 divided by k . And I will write this as half square root of ζ divided by square root of ω_n by k , if you know the damping factor. And the natural frequency second-order system you can make statements of about the kind of step response going to have. You know that if the

damping factor is much, much more than one the step response looks like the step response of a first order system. And if the damping factor is much less than one there will be sinusoidal ringing in the step response. The damping factor characteristics step response and tells you whether the step response is over damped, critically damped or under damped.

(Refer Slide Time: 35:37)



So, a negative feedback amplifier with an extra pole in forward path, this as a second order transfer function whose d c value is k as you expect it is the ideal value. And the natural frequency of this is square root of p_2 time ω_u by k and the damping factor is half ratio of p_2 by ω_u by k and the square root of the whole thing.

Now, if you plot the step response of system like this, response of the system to unit step. So, let's say the input as a unit step. Now, what will happen after a long time the output will be equal to the d c gain of the system times the input voltage. So, after a long time the output is going to reach k volts, because the input is one-volt the output is going to reach k volts after a while.

Now, exactly how it is gets there is determined by the damping factor, if the damping factor is much more than 1, then you get a very slow lag in response like that. And if the damping factor is much less than 1, we will get a response that overshoots and under shoots and ringing is a lot and goes that way. This is what is known as an under damped

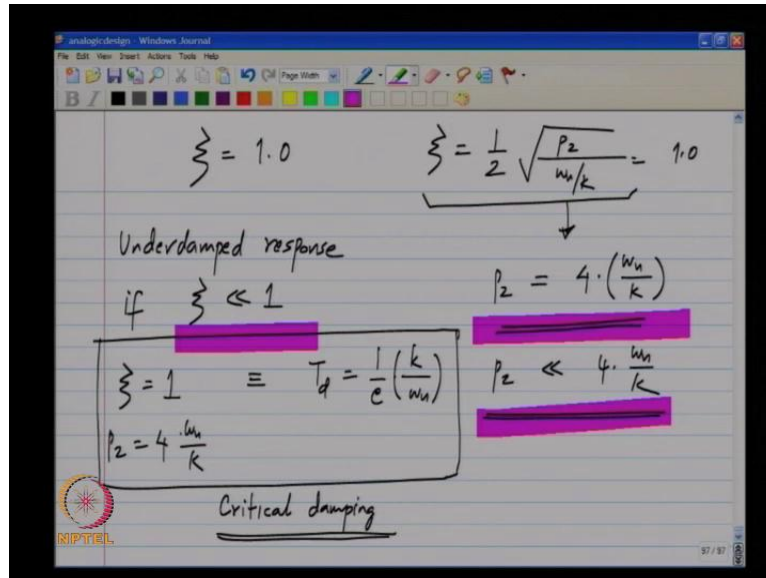
response and if the damping factor equals one you get the fastest possible response without overshooting. And this is equivalent to a critically damped response.

So, what would you like to have is usual critical damped response or maybe a slightly under damped response, there is little overshoot. Normally would not like to have something that is shown here which has a lot of ringing, you would like to have just a little overshoot if at all there is some. So, this is acceptable, if it starts are like that, but certainly something like this that rings many times is not acceptable.

Now, if you recall the analysis the date break the delay in the feedback loop, we saw that we had a similar phenomenon for small values of delay the response actually speed up that is lets saying, for modest values of damping factor which are greater than one the response actually speeds up. If the damping factor is much more than one the response is rather slow. And if the damping factor approaches one the response become faster and faster and the response at damping factor one is to be similar to the response for the delay being $1/e$. The normalized delay being $1/e$ that is critically damped that is it is fastest response you can get without overshooting.

Now, damping factor values that much less than 1, seem to produce responses that are similar to one that delays much more than $1/e$ you start to get ringing and overshoot and so on. What we will do in next is to relates this to see how that delay a comes about because of the extra pole. The desire response is usually critically damped or slightly under damped. So, this is kind of response that we are looking for. So, first let us calculate the value of parasitic poles that we permissible to have this.

(Refer Slide Time: 40:39)



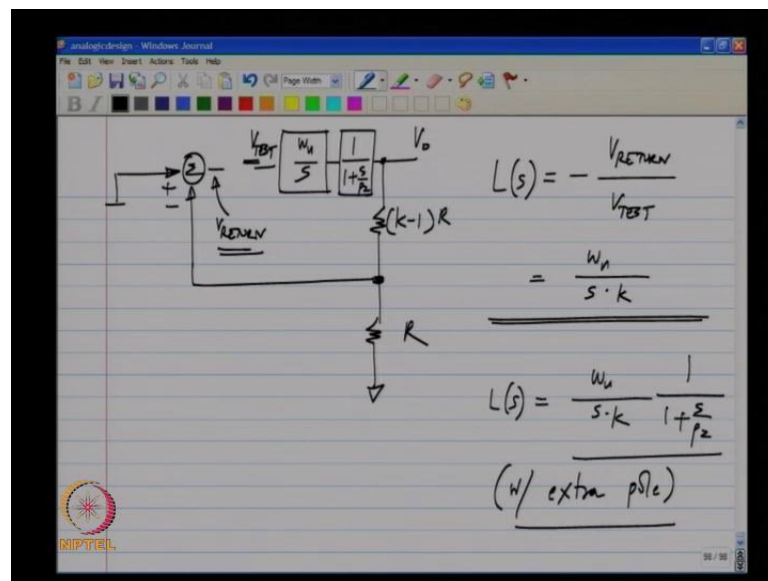
Let us say I want to have a critically damped system that is I would like to have zeta equal to 1.0. So, this means that zeta which is half of a square root of p_2 by ω_u by k this should be 1.0, and from this you see that p_2 as to be equal to four times ω_u by k . We also know that we get an under damped response if zeta is much less than 1; that means, that if p_2 is much smaller than four times ω_u by k we can work out the any quality from this formula, if p_2 is much smaller than four-times ω_u by k you will end up with a severely under damped response.

So, you would like to keep p_2 somewhere in this range, where you will get either critical damping or a slight under damping, but certainly not a severe under damping. So, you can associate this values zeta equal to 1 is roughly like T_d being 1 over c k by ω_u . And zeta equal to one corresponds to p_2 being four times ω_u by k . We see that we can have high frequency of poles, that is not per say problem, if you look at this particular polynomial the denominator as a coefficient which always positive.

So, that means, that this system is always stable the roots of the denominator will always be in the left half plain, which means that the natural response dies out of the sometime. So, this is system is unconditionally stable, we can have any value of p_2 this is system is stable, but the problem is that if the second pole happens to be at very low frequency, that is if p_2 is much smaller than four times ω_u by k , you will get is severely under damped response because the damping factor zeta because much smaller than 1.

So, the summary of the system with one extra pole is that you can have the pole it does not cause instability, but it can cause severe under damping. What will do next, what we will do next is to extend the analysis to higher order system as we get higher and higher order the analysis becomes more and more complicated because you will have more complicated polynomials. What we will do is we will have a let's say 2 extra poles at an identical location than three extra poles and see what happens, but before we do that let's look at what happens to the time domain response many have extra pole.

(Refer Slide Time: 44:17)

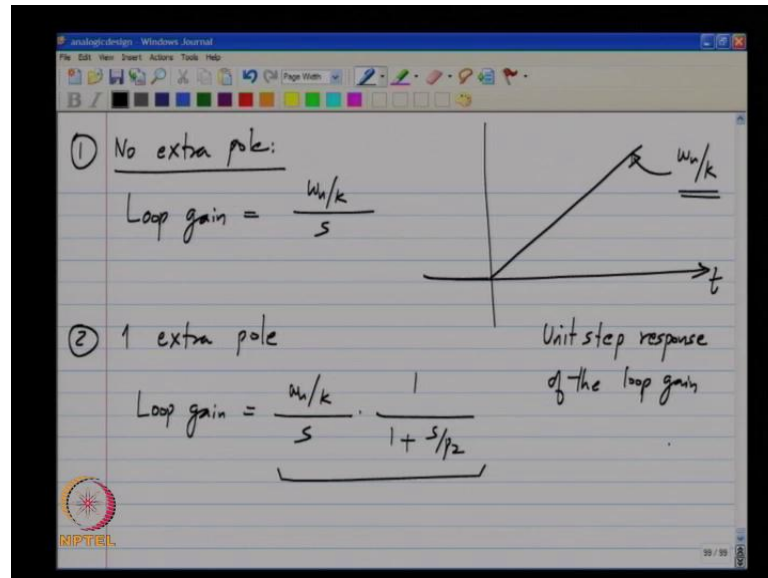


This is the system which by now is very, very familiar. Now, I said earlier that to quantify the amount of negative feedback, we use the term loop gain, which is we said the input to 0, you break the loop and you apply some touch signal, and see what comes back here. This is the loop gain that quantifies the amount of negative feedback and if the amount of negative feedback is very large the system behaves ideally, as you expect you would like to have as large negative feedback as possible.

In this particular case the loop gain is if you apply V_{test} here V_{test} of times ω_n comes there and then that divided by k comes here a negative of that comes, and the minus sign included in the definition of loop gain. So, L of s defined to be minus V_{return} by V_{test} which happens to be ω_n by s times k . Now, this is for the system without any extra pole. Now, if you have an extra pole here it is very easy to analyze, we get an extra factor of $1 + sT_n$ added on to our original loop gain L of s is simply

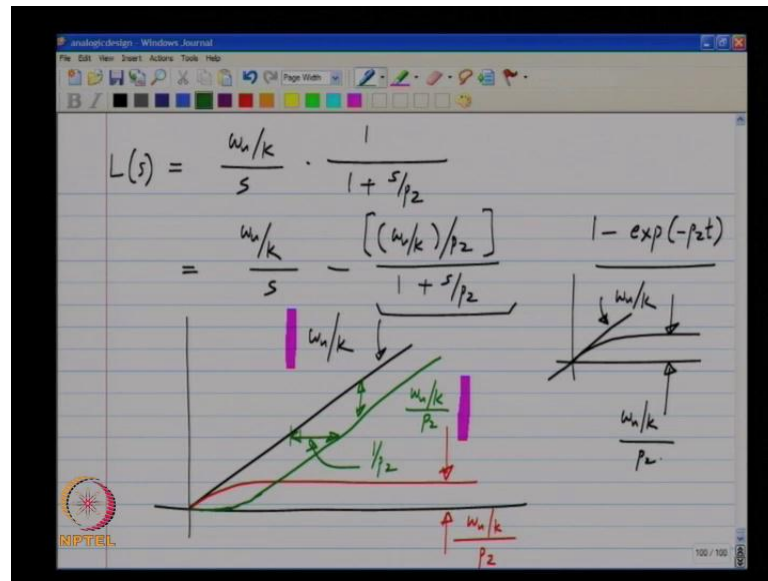
turn out to be ωu by s times k 1 by 1 plus s by p 2 this with the extra pole. So, what we can do now is to compare the time domain responses of the loop gain and see how they behave.

(Refer Slide Time: 47:06)



This is the loop gain with no extra poles and here I will plot the unit step response of the loop gain. And the unit step response of this function is very easy, it is a ramp this is time the unit step response a ramp and the slope of the ramp is ωu by k . Now, let us say we have one extra poles than the loop gain will be ωu by k divided by s 1 by 1 plus s by p 2 . Now, to study the step response of this we can expand this in partial fraction.

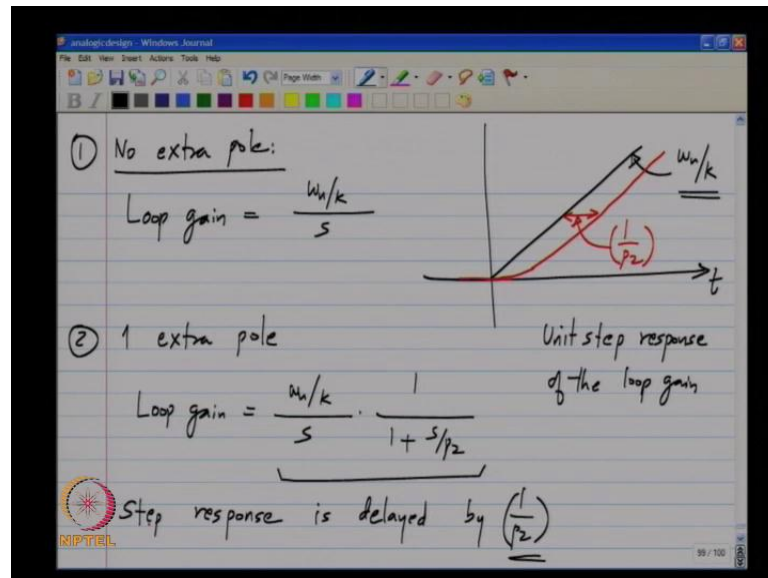
(Refer Slide Time: 48:36)



We can expand the loop gain in the partial fraction form it can be rewritten as. So, we can verify for yourself that this coefficient satisfy the equation, satisfy the expression for loop gain. Now, the reason to write it down as a in the partial fraction expansions is now the step response of loop gain, the step response of first part of it minus the step response of second part of it. The step response of the first part we already know it is a ramp whose slope is ω_u/k and the step response of second part is a step response of first-order system, which as the form $1 - \exp(-p_2 t)$, it as this particular shape.

And because of this particular factor the height of this will be ω_u/k divided by p_2 and slope at the start will be exactly equal to ω_u/k . So, that means that we have 2 subtract something like this from black curve, and both of them have the same initial slop, and the height of this is ω_u/k divided by $k p_2$. And if you take the difference between these the starting slope will be 0 and then built up, and after while there is constant difference between the 2 poles. And the constant differences ω_u/k by k divided by p_2 and we can also expressed it as a constant difference in the horizontal direction. And the difference in the horizontal direction is nothing but difference in the vertical direction divided by the slope. So, the difference in the horizontal direction is nothing but $1/p_2$.

(Refer Slide Time: 51:20)



So, plotting into on this axis here if I have an extra poles p_2 and I get a which as some detail here which I am going to ignore for now, but in the long-term simply horizontal shifted compare to the ideal response and the horizontal shift equals $1/p_2$. So, approximately speaking that step response with extra pole is delayed compared to the one without the pole by an amount $1/p_2$.

So, it is no surprising that there result when you have an extra poles look similar to result when add ideal delay, we also saw that if the delay becomes very large that is if the value of $1/p_2$ becomes very large or p_2 becomes very small, you will have severe under damping and sever ringing. So, having a pole is roughly equivalent to delay and having multiple poles you will have delays to each pole and you will have to add them up. And will discussed that as we gone higher order systems.