

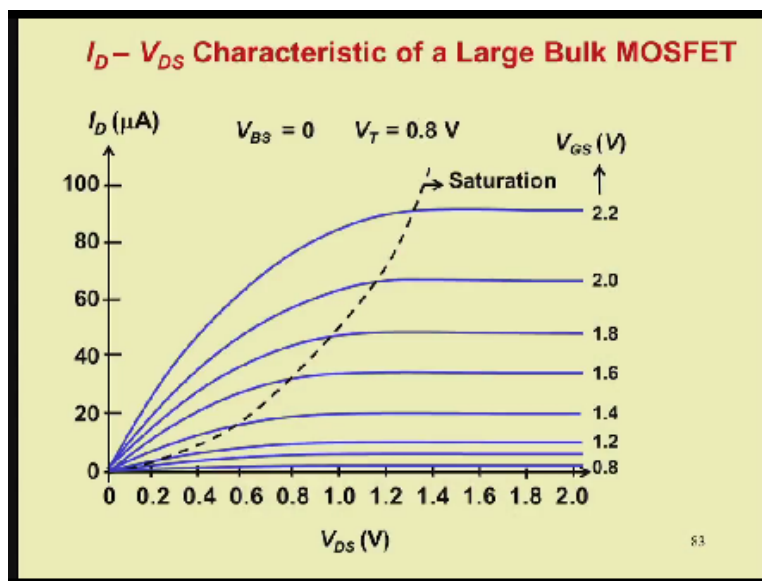
Semiconductor Device Modeling
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Lecture - 43

DC Model of a Large Uniformly Doped Bulk MOSFET: Qualitative Theory

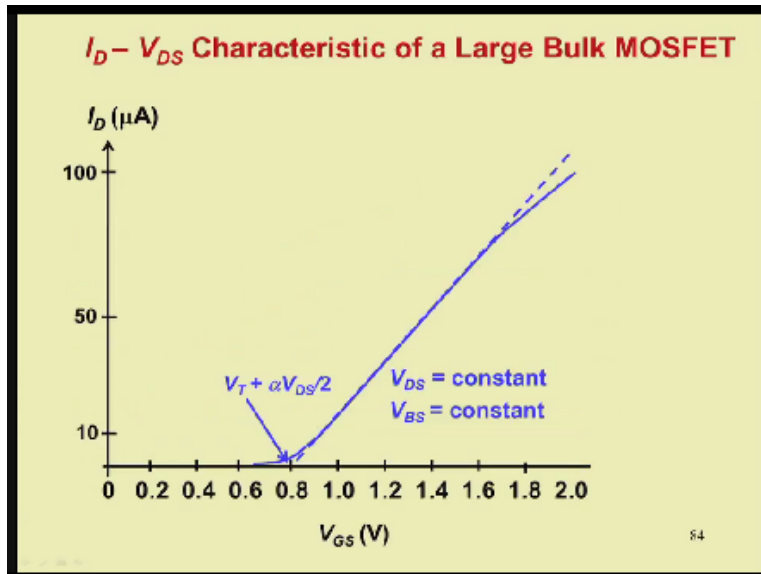
Let us continue our discussion on the qualitative theory underlying the DC model of a large uniformly doped bulk MOSFET. Now so far we have done the following.

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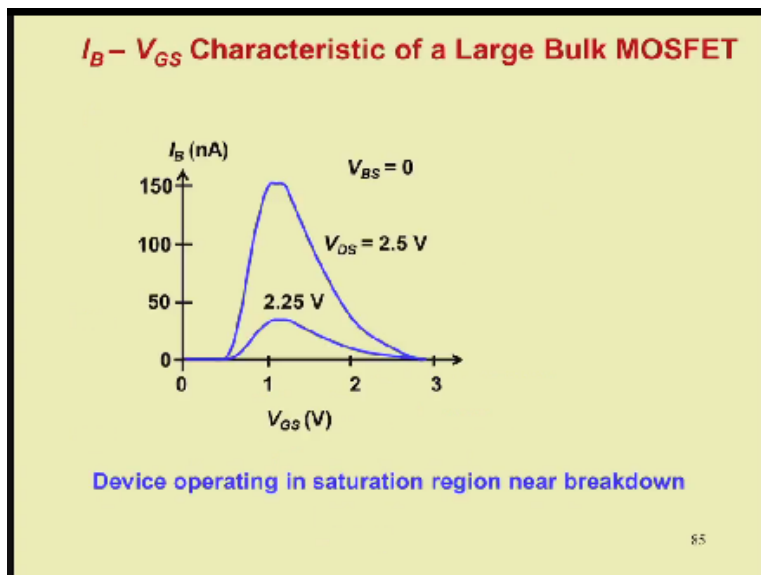


We have explained the shape of the $I_D - V_{DS}$ curves and things such as why the current saturates beyond some point, why does the saturation voltage go on increasing and below saturation, why do the current rise rapidly for small values of V_{DS} .

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Then we explained the shape of the $I_D - V_{GS}$ curve where the current is plotted on a linear axis.
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Then we explained the shape of the $I_B - V_{GS}$ curve where I_B is the substrate current. Now this curve corresponded to device operating in saturation region near breakdown.
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Module 10

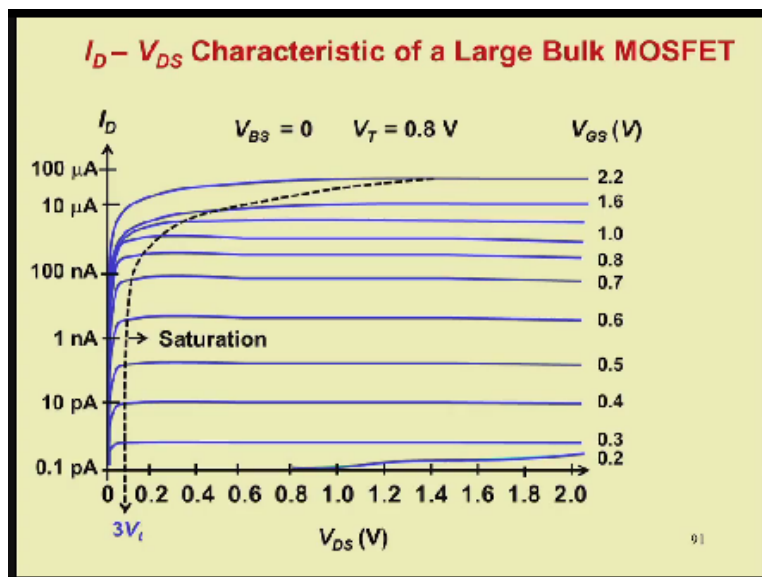
DC Model of a Large Uniformly doped Bulk MOSFET: Qualitative Theory

- Shape of the I_D - V_{DS} and I_D - V_{GS} curves
- Factors responsible for creation and continuity of J_n , J_p , E
- Factors responsible for boundary conditions on (n or J_n), (p or J_p), (ψ or E)
- Flow lines for J_n , J_p , E and equi-potential lines for ψ

In the present lecture, we shall do the following. We shall consider some other features of the shape of the I_D - V_{DS} and I_D - V_{GS} curves. Specifically, we will consider the sub-threshold region and the breakdown region and explain the I_D behavior in these regions. Then we shall consider the factors responsible for creation and continuity of J_n , J_p and E . We will consider the factors responsible for boundary conditions on n or J_n , P or J_p , ψ or E .

Finally, we shall sketch the flow lines for J_n , J_p , E and equi-potential lines for ψ .

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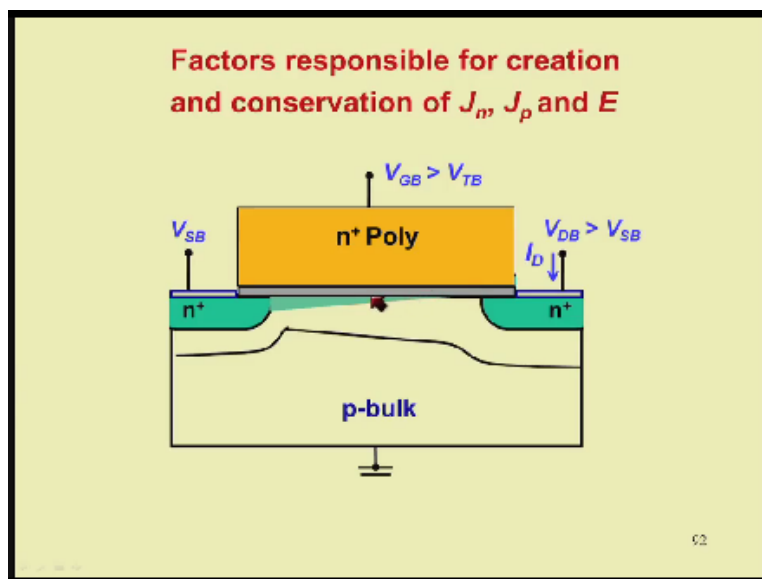
Let us begin with the I_D - V_{DS} curves with I_D plotted on a log scale. On this semilog plot, the region below threshold gets amplified. Here the threshold voltage is 0.8 V and therefore, this is

the curve corresponding to threshold, $V_{GS} = 0.8$ and this region is a subthreshold region. Now one can distinguish the subthreshold region from the superthreshold region in terms of 2 features.

One is that in the subthreshold region, the current seems to be increasing exponentially with V_{GS} because I_D is on a log axis and increments in I_D on the log axis seem to be uniform for uniform increments in V_{GS} . In the superthreshold region, however, the current does not increase uniformly with uniform increments in V_{GS} . Now the second feature is that in subthreshold region, the current seems to saturate at approximately 3 times V_T for all values of V_{GS} .

So the saturation point seems to remain constant independent of V_{GS} . Whereas in superthreshold region, the saturation voltage seems to increase as V_{GS} increases. Now the fact that these 2 features distinguish the subthreshold and superthreshold regions mean that a mechanism of current flow in superthreshold region is different from that in the subthreshold region. Now let us understand this point by looking at the charge conditions in a MOSFET.

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In superthreshold, that is when $V_{GB} > V_{TB}$, the inversion charge in the MOSFET is large. Here we have shown the inversion charge conditions from source to drain and the depletion charge conditions, also from source to drain when the usual biases are applied to the MOSFET. Now there is an electric field from drain to source; therefore, there is a drift current and there is a

gradient of the inversion charge from source to drain. Therefore, there is a diffusion current as well.

Now when $V_{GB} > V_{TB}$, inversion charge is significant and therefore, the drift current is large and dominates over the diffusion current, because the drift current depends on the inversion charge, it is proportional to the charge whereas the diffusion current is proportional to the gradient of the charge. So because the charge itself is large, the drift current dominates over the diffusion current.

On the other hand, if you go to subthreshold region, V_{GB} less than V_{TB} , the inversion charge is very small and therefore, the drift current which is proportional to this charge is drastically cut down. However, there is a charge gradient from source to drain and therefore, the diffusion current becomes more significant than the drift current. So in subthreshold region, the mechanism of current is predominantly diffusion; in the superthreshold region, it is drift.

Now, if the mechanism of current flow is diffusion, let us see why this current should saturate when the drain to source voltage is more than 3 times V_T . Now I want to remind you that the curves that we saw corresponded to $V_{SB}=0$. So we shall therefore find that the drain to bulk voltage would be the same as drain to source voltage, right, if you ground this. Now the MOSFET in subthreshold region in certain ways is analogous to a bipolar transistor.

So since the current here from source to drain is because of the diffusion, the situation is analogous to that in a n-p-n bipolar transistor where this is the emitter and this is the base region and this is the drain region and this is the injected electron concentration from emitter which falls as you move towards the collector. Now you will recall from junction theory, that in a bipolar transistor, the charge concentration near the emitter depends on the emitter base bias and the charge concentration near the collector depends on the collector to base bias.

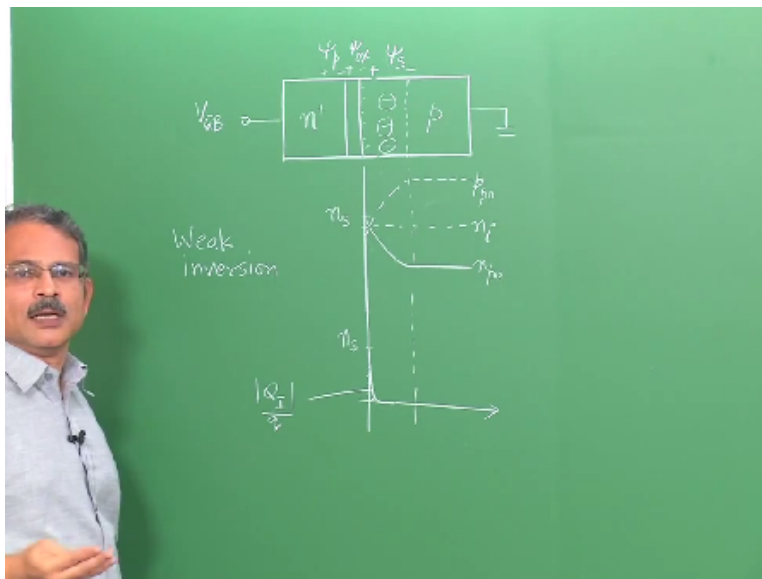
So by analogy, we can say that the charge concentration at the drain end in the MOSFET depends on the drain to bulk reversed bias. Now once the drain to bulk reverse bias is more than 3 times V_T , from the junction theory you know that the charge concentration here, the electron

concentration or minority carrier concentration in the p base would be really small and therefore beyond reverse bias of 3 times V_T across this n+p junction, there is really no significant change in the charge concentration.

It is already very small and therefore, the current from this end to the other end saturates. So this is the reason why in subthreshold region, the drain to source current, okay, that is the current flowing from here to here, the electrons flow from source to drain, so this current saturates, this current is because of diffusion and it saturates for reverse bias across the n+p junction of 3 times V_T or more.

So this is how we can explain the saturation of the current at approximately 3 times V_T independent of V_{GS} , okay. So the V_{GS} is going to change the inversion charge concentration near the source, but at the drain end, the inversion charge will depend only on the drain to bulk bias as we have discussed. So because inversion charge concentration increases at the source, the current increases. Now let us explain why the current should increase exponentially with respect to V_{GS} .

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Now let us start with a 2-terminal MOSFET in subthreshold region. Now the applied gate to bulk bias falls partly across the poly region here and partly across the oxide and partly across the semiconductor or silicon and you have a depletion region. Now since we are considering

subthreshold, there are 2 possibilities. You can have either only depletion or you can have weak inversion.

Let us consider weak inversion because unless we have some inversion charge, we will have no current between source and drain when we attach source and drain to this 2-terminal device. Now how does this inversion charge vary with V_{GB} , that is a question. Let us sketch the electron concentration on the p side. So this would be something like this. Now since it is weak inversion, the electron concentration at the surface n_s would be more than n_i , but it would be less than the hole concentration in the bulk. So this is the hole concentration.

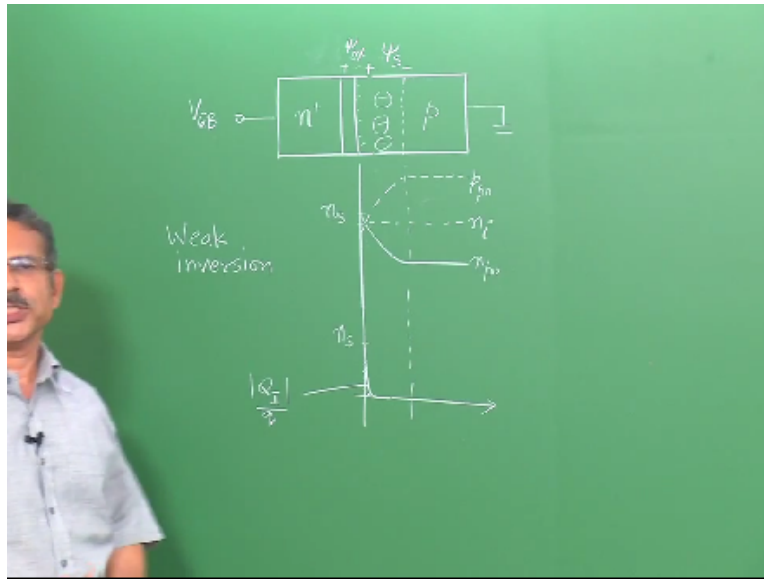
So let us write that we are considering weak inversion. Now you know that the n_s varies exponentially with ψ_s . This is from the Boltzmann relation. So therefore, if you know ψ_s varies with V_{GB} , you can interrelate n_s to V_{GB} and then therefore we can get the relation between the inversion charge and V_{GB} . Now n_s is the volume concentration of electrons whereas when we talk about inversion charge, normally it is per unit area of the gate.

So let us show that to show the inversion charge q_i , we sketch the same curve on a linear scale, that would look something like this. On a log scale, it decreases at certain rate, but on a linear scale, you know, the fall is very rapid, we have discussed that log and linear scale representations of the carrier concentration. This scale has to be log here because I am showing the hole concentration and the electron concentration both and you know that the difference between these 2 is several orders of magnitude, okay.

Now, this is your n_s , this one is the linear representation of the same curve. Area under this electron concentration is actually the inversion charge. So this we can show as q_i/q . I will put a modulus here because this area is positive whereas inversion charge is negative. Now q_i to a first approximation is proportional to n_s , because you can see that this shape of the shaded area is almost like a triangle and therefore, the area under the triangle will be proportional to the height of the triangle that is n_s .

So therefore we can say, this q_i or inversion charge varies approximately exponentially with this ψ_s because n_s varies exponentially with ψ_s according to Boltzmann relation. Now let us relate ψ_s and V_{GB} . Now in strong inversion, you know that the ψ_s is saturated, right, at approximately 2 times from a level plus 6 times the thermal voltage. So once the ψ_s has saturated, if I increase V_{GB} , then the increment in V_{GB} will be absorbed into increment in ψ_{ox} .

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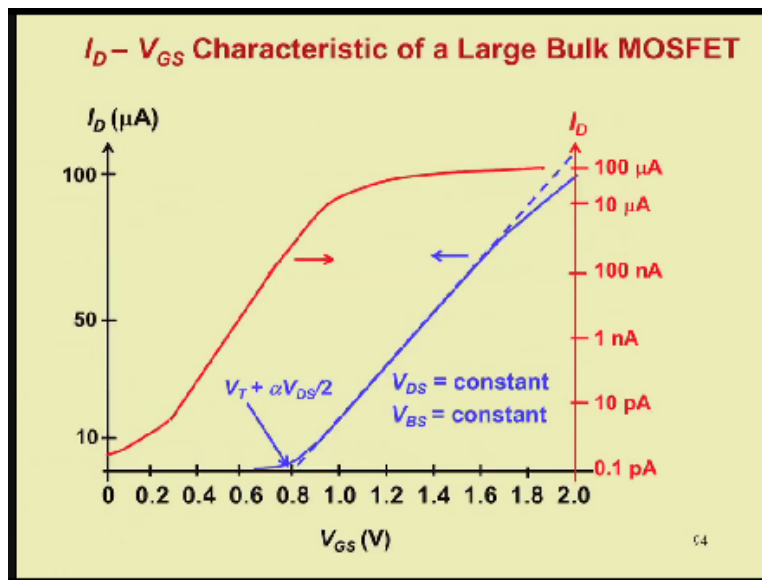
Let us for simplicity neglect ψ_p , okay, so I will remove ψ_p from here. So there is almost no change in ψ_s when you increment V_{GB} , the entire increment appears across the oxide, ψ_{ox} . In subthreshold, however, when you increment V_{GB} , that increment will be absorbed into ψ_{ox} as well as ψ_s . I want to emphasize that we are ignoring the ψ_p , potential drop across the poly. Therefore, now we can see why the inversion charge increases exponentially with V_{GB} .

If ψ_s increases linearly with V_{GB} , then imminently n_s will increase exponentially with V_{GB} because the n_s increases exponentially with ψ_s and since q_i is proportional to n_s as shown here or as shown here; therefore, q_i will increase exponentially with V_{GB} . Now at this point, we cannot exactly show how ψ_s varies linearly with V_{GB} . All that we can say is that when you are increasing V_{GB} in the weak inversion region, the depletion width is expanding, okay.

The depletion width has not saturated and expansion of the depletion width means expansion of ψ_s or increase in ψ_s . So since ψ_s keeps increasing with V_{GB} ; therefore, n_s also keeps increasing with V_{GB} . So we can in a loose way say ψ_s , if it is assumed to be proportional to V_{GB} , then n_s will increase exponentially, okay. So this is how we can explain the exponential behavior of the inversion charge as a function of V_{GB} in subthreshold or weak inversion region.

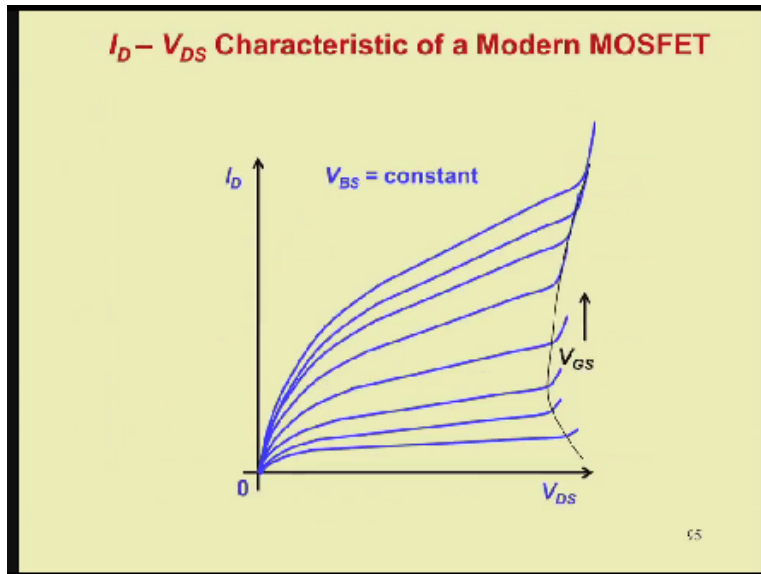
Now we have remarked that the current from drain to source in subthreshold region is because of diffusion, okay. Now diffusion means gradient of the inversion charge. So since the inversion charge itself varies exponentially with V_{GB} , the gradient also varies exponentially with V_{GB} and therefore the current varies exponentially with V_{GB} . So this explains why the current in saturation, okay, the drain current in saturation in a MOSFET increases exponentially with V_{GB} .

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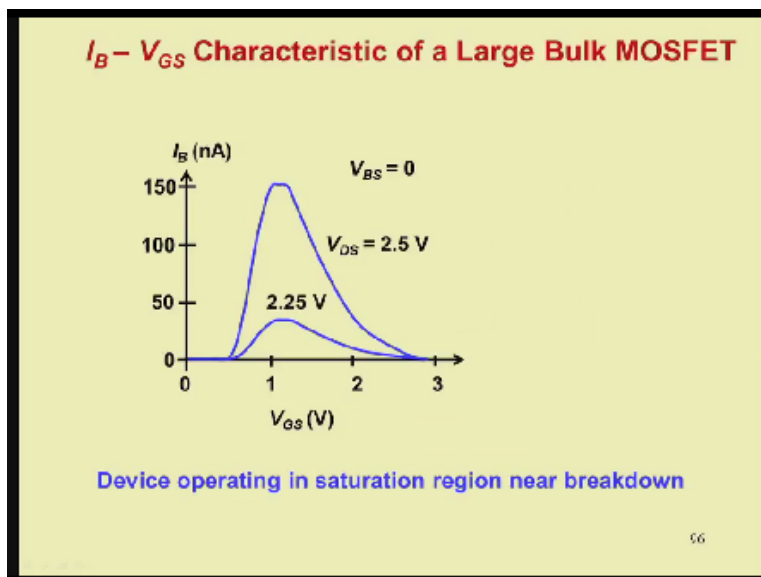
Now this explanation would also apply to the $I_D - V_{GS}$ curve where I_D is plotted on a log scale, that is the red curve. So the reason I_D appears as a straight line over a significant part of the subthreshold region on this graph is because I_D varies exponentially when V_{GS} near threshold or in subthreshold region.

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Now we shall briefly touch upon the MOSFET breakdown. When we showed the long channel MOSFET curves or the curve corresponding to $I_D - V_{DS}$ curve corresponding to a large MOSFET, large bulk MOSFET, we did not show breakdown because breakdown voltage of a large bulk MOSFET is really very high. So the breakdown is of interest in a modern MOSFET which is of a small size.

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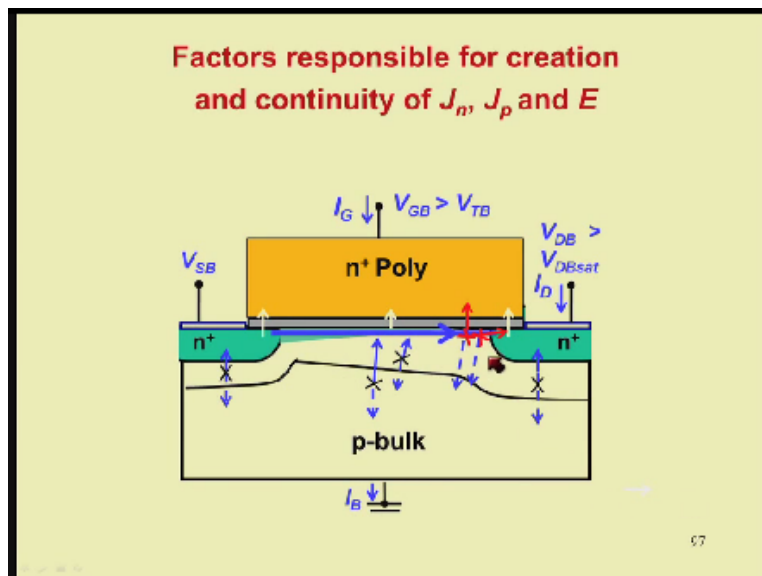


So detail consideration of this is more appropriate when we take a up modern MOSFET; nevertheless, we shall touch upon this topic because the behavior of the breakdown voltage with V_{GS} is related to the behavior of the substrate current with V_{GS} which we have explained already. Since this is a $I_D - V_{DS}$ curves corresponding to a modern MOSFET, you see that the

current is not saturating to that extent because there are certain phenomena which are particular to a small geometry device.

And these aspects, however, we will not touch upon now because now we want to concentrate on the large bulk MOSFET. Now let us explain why the breakdown voltage should decrease when you increase the VGS from threshold voltage onwards, but beyond some gate source voltage, the breakdown voltage increases. Let us recapitulate the reasons for the shape of this ID-VGS curve. No what we remark was that the substrate current I_B is due to impact ionization near the drain in a MOSFET.

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So near the drain, what is happening is that the electric field is large and therefore, this electric field multiplies the electrons which are moving from source to drain. So the current that results from this phenomenon, will be proportional to the source of electrons, namely, the I_{DS} as well as the multiplication factor which depends on the electric field magnitude near the drain. So we should consider both the magnitude of the electric field near the drain and the magnitude of the I_{DS} .

If anyone of them is small, then the current that results from this impact ionization will be small, okay. So based on this consideration, we can explain why the current is small for small for small values of VGS and large values of VGS. For small values of VGS, the inversion charge is very

small and therefore I_{DS} is small. Note that for V_{GS} less than V_t , this point is V_t , so V_{GS} is less than V_t , inversion charge is almost negligible and current is negligible, okay.

And therefore the I_{DS} is small and therefore even though the multiplication factor maybe large because electric field near the drain is large, current is small. At high values of V_{GS} , what happens is, that the inversion charge is large and therefore the field which was restricted near the drain for small inversion charge gets spread over the entire channel length, okay. It becomes more uniform over the entire channel length and therefore, its magnitude decreases for a fixed value of V_{DB} .

And this decrease in magnitude of the electric field, it is responsible for decrease in the current even though the source of I_{DS} is large, or rather the source of electrons which can multiply is large, the multiplication factor itself is small here, okay and in between you have peaking of the current because here in this range, the I_{DS} which supplies the current for multiplication is reasonably high and the electric field also is reasonably high which can multiply the current.

Now applying the same explanation here, when V_{GS} is small, your I_D is small and therefore, you need a large value of V_{DS} to increase the electric field to a value where the small current can be multiplied to a significant extent and it will cause avalanche breakdown. When you increase your I_D , the current can be large even with a smaller multiplication factor and therefore at the smaller value of V_{DS} because even with a smaller electric field, you can get a large amount of current.

Now for very high values of V_{GS} , the field tends to become more uniform over the channel length and it decreases and therefore, unless you increase the field, you cannot get reasonable multiplication and that can only happen by increasing the value of V_{DS} . So that is why for high V_{GS} again, the breakdown voltage increases. Now let us summarize the factors responsible for creation and continuity of J_n , J_p and E .

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Factors responsible for creation and continuity of J_n , J_p and E

| Flow | Creation | Continuity |
|-------|--|---|
| J_n | by drift + diffusion of the inversion charge | <ul style="list-style-type: none"> • current sources due to thermal gen. and impact ion., and sink due to tunneling are neglected • steady state (charge conc. does not change with time) |
| J_p | neglected | neglected |
| E | by applied / built-in potential differences | space-charge sources / sinks field lines |

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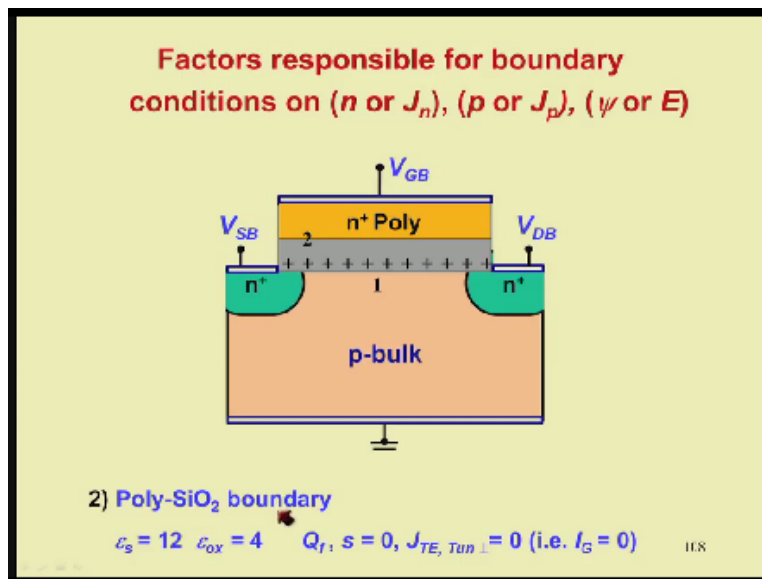
Let us look at J_n , this is created by drift as well as diffusion of the inversion charge. In the continuity column here, we need to make a list of the sources and sinks of the electron current. Continuity is same as conservation. So we make the statement that current sources due to thermal generation and impact ionization and sink due to tunneling are neglected. So let us go back to the diagram to understand this. You can see that you have thermal generation in the depletion region and also within a diffusion length from the depletion region.

So the electrons from these generation centers are all moving towards the drain and they are contributing to the drain. Similarly, there is impact ionization near the drain and this is also contributing electrons. Now there is some loss of electrons to the gate because of tunneling, right. So therefore tunneling is like a sink whereas impact ionization and thermal generation are like sources of electrons. So that is what we have said here. Another point to note is that it is steady state situation which means the charge concentration does not change with time.

This also has to be taken into account in the conservation or continuity of electrons. Now we are neglecting the hole current altogether. So we do not bother about creation and continuity of J_p . Coming to the electric field, the electric field is created by applied or built-in potential differences. So you look at the diagram here, we are applying gate bias, source bias and drain bias with respect to bulk and you have work function differences between n plus poly and p bulk.

And similarly, you have work function differences or built-in potentials between source and bulk and drain and bulk. So all this will be responsible for the electric field. Now as far as continuity of electric field is concerned, this is decided by the space charge which sources or sinks field lines. Going back to this diagram, the space charge here is because of inversion charge and where as depletion charge. So these are the charges which are responsible for sinking of field lines or sourcing of field lines.

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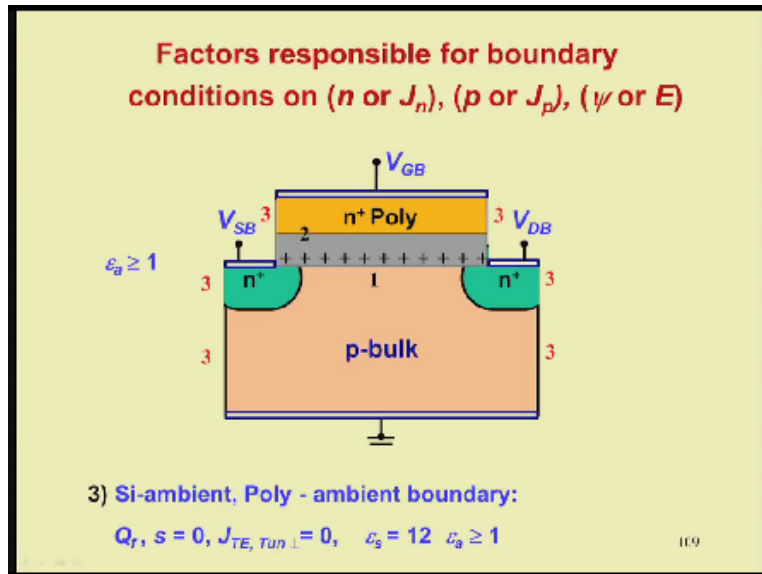


Now let us consider the factors responsible for boundary conditions on n or J_n , p or J_p & ψ or E . Here is the diagram of the device where we have clearly shown the electrodes. This is the bulk electrode, this is the source electrode, this is the drain electrode and this is the gate electrode. The first boundary of interest which is also the most important boundary in this device is the silicon dioxide silicon interface. Now at this boundary, the conditions will be governed by the following factors. Dielectric constant of silicon is 12 that is dielectric constant of this region.

The dielectric constant of oxide is 4 that is the dielectric constant of this region. Q_f is not 0, so there is an interface charge, okay, fixed charge of positive polarity. However, the surface recombination velocity is 0, then the thermionic emission current density and the tunneling current density. these are 0 because $I_G = 0$. So this is another important consideration that there is no current flowing perpendicular to this interface, okay.

Next, we look at the poly in silicon, silicon dioxide boundary, that is boundary number 2 here. The factors responsible for conditions at this boundary are silicon dielectric constant is 12, oxide dielectric constant is 4. Unlike this interface, at this interface, you do not have any fixed charge. So Q_f is 0. Surface recombination velocity is 0 and as we have remarked in the previous slide, thermionic emission and tunneling currents perpendicular to this interface are 0.

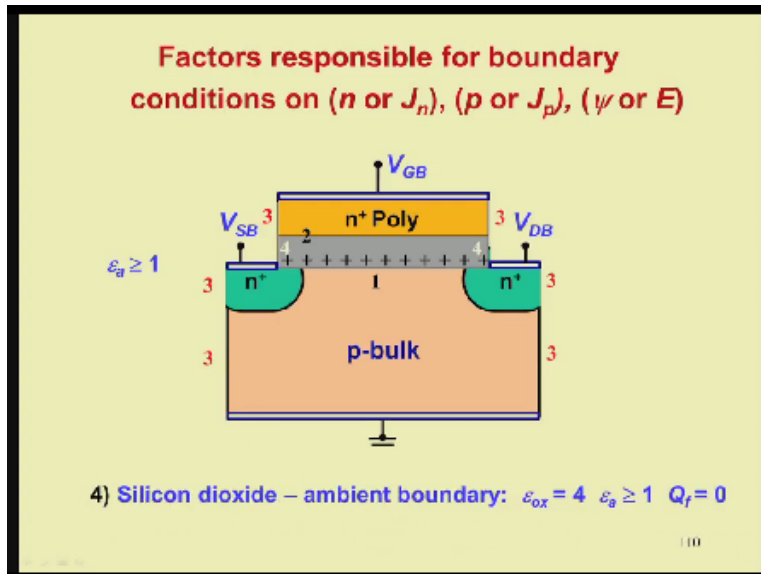
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The third boundary is a silicon ambient and poly-silicon ambient boundary. So this is the silicon ambient boundary, here, similarly here and here, you have the poly-silicon ambient and poly-silicon ambient boundary at this ends. Now the important considerations here are Q_f and surface recombination velocity are 0 at this boundary and there is no thermionic emission or tunneling currents perpendicular to this boundaries.

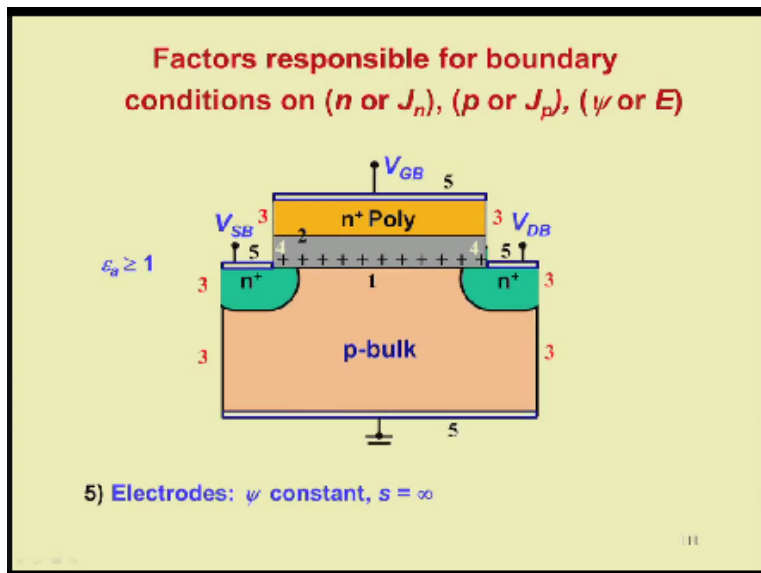
The dielectric constant of silicon whether you poly-silicon or crystalline silicon, it is assumed to be 12 and the dielectric constant of the ambient is more than or = 1. The ambient is all of this. So here the dielectric constant is more than or = 1 because the ambient can be air or vacuum in which case the dielectric constant would be 1 or it could be some other material, such as silicon nitride or silicon dioxide, right, which can be coated around this device. So therefore, in that case the dielectric constant would be more than 1.

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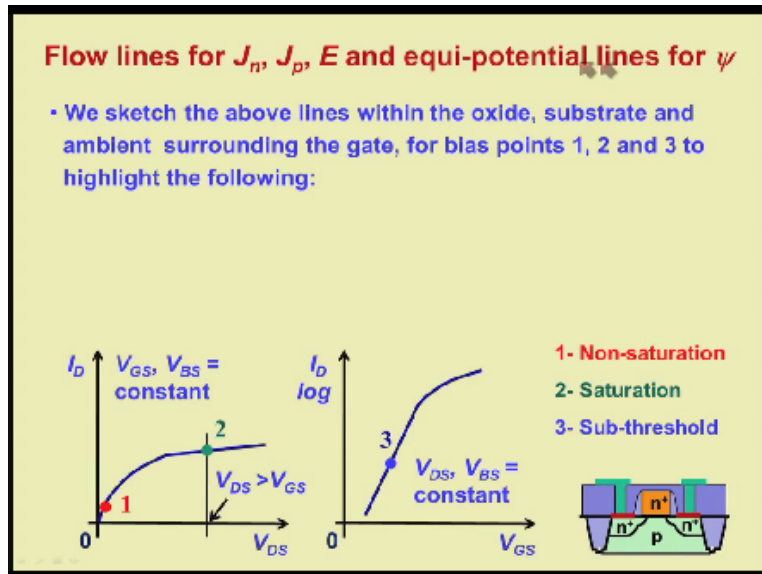
The 4th boundary is silicon dioxide ambient boundary, that is here and here. The factors at this boundary are the oxide dielectric constant = 4, the ambient dielectric constant ≥ 1 and there is no fixed charge at these boundaries.

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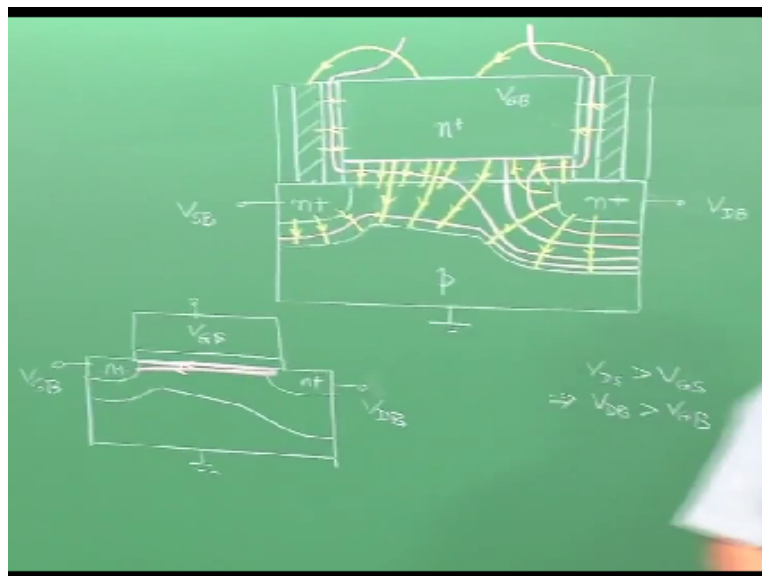
Finally you have the electrode boundaries and at these boundaries, the potential is constant and surface recombination velocity is infinite. This means for example, if you take this electrode, all over this, the potential will be uniform and S is infinity which means the electron and hole concentrations at this boundary will be equal to their equilibrium values.

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Now let us sketch the flow lines for J_n , J_p , E and equi-potential lines for ψ . This is our device structure.

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Now we shall sketch the lines on the board. Now notice that I have simplified the junction boundary for source and drain as compared to the boundary shown here, okay. Similarly, I have just assumed this ends to be vertical, this is again for simplicity. Now let us show the metal contacts on either side of the gate. In between the metal and the gate, we will assume this to be an insulator. I am not going to show the different insulators associated with the spacer and isolation regions. We will just show one insulating region here.

Further, we will assume that the top surface is coinciding with the top of the n plus gate okay and so the picture would be as follows. So I am assuming a insulator here and an insulator here. Then I put the metal, and here too. Here you have the insulator and this is the metal. Now the bulk is grounded, this region is the same as the drain, right. So let me show the potential on this side because I would like to draw field lines and so on here.

This is V_{DB} , is V_{SB} and here, you have V_{GB} , I will show it on in the gate region because I would like to use this to draw some field lines. Now there is a structure in which we want to show the various lines. Now we shall sketch these lines within the oxide substrate and ambient surrounding the gate for bias points 1, 2 and 3 shown in the diagram below. So bias point 1 is in non-saturation in the linear part of the I_D - V_{DS} curve, so the V_{DS} is very small.

The bias point 2 is in saturation region with $V_{DS} > V_{GS}$. This means that V_{DB} will be $> V_{GB}$, so $V_{DS} > V_{GS}$ is same as $V_{DB} > V_{GB}$ and the bias point 3 is in subthreshold region, here, okay. Now I will leave it to you as an exercise to sketch the various lines for bias points 1 and 3 and I am going to sketch the lines for bias point 2. Let me first show the depletion region. Let us first sketch the equi-potential lines.

Since the drain voltage is more than the gate voltage, if I move along the channel, at some point between the drain and the source, I will have the voltage equal to the gate voltage. So this is an equi-potential line corresponding to V_G and this is a point which has the same potential as this; therefore, from here, I could join this and show equi-potential line like this. Now when I move into the substrate, I can extend this equi-potential line as follows, something like this.

Now let us take an equi-potential line in the oxide, somewhere here let us say starting from somewhere here. Now, this potential is a same here and therefore this potential will be in between this potential and this potential and therefore along the channel if I move somewhere at this point I will get a potential between these 2 potentials which is same as this; therefore, this equi-potential Line would go something like this and then if I extend it here, it would be something like.

Let us take an equi-potential line here, now let me use a different color for this line so that the things are clear. Let us take an equi-potential line in between within the oxide here. So let me start from here. Now a point between these 2, somewhere here, will have the same potential as this point which is between these 2. So this line would be something like this and then it will go like this. Now if I take an equi-potential line between the depletion edge and the n plus source, that would be something like this, something like this.

Now let us extend this equi-potential line into this region which is an insulating region. Now it will extend something like this, because potential of this region is the same as this region and therefore, this potential lies between this potential and this potential which is same as this potential and this potential. So therefore here, you will get a equi-potential line parallel to these 2 surfaces. I can extend the equi-potential line here too like that, it will be like this.

Now based on these lines, let us now sketch the electric field. Note that our device is in strong inversion and therefore, there will be a lot of inversion charge apart from the depletion charge that is shown and in fact most of the field lines from the gate would terminate on this inversion charge and there will be a few lines which however will extend into the depletion region. So the field lines have to be perpendicular to the equi-potential line, so that would be something like this.

So here, this line should be perpendicular to that line. Here on the other hand, the field will be from substrate to gate because this potential is more than this potential. So in this region, potential here is less than potential here. So the picture is like this, this line would be something like this, so maybe it is going deeper inside. So let me show some lines terminating on the depletion charge.

Here you will have lines terminating like this and here similarly, you have lines like that. Here the lines would be directed from drain to gate because drain is higher than gate. Here the lines will be directed from gate to source because gate is more than the source in potential. Now here you will have line something like this. Now note that whatever field lines we are showing here,

correspond to the particular surface that we have assumed, okay, the particular method of termination of this drain and source contact and so on.

This may or may not correspond to the real situation. In reality, you may have many other things of the top and they will decide the field lines, okay. So I am showing the field lines for this hypothetical case so that you understand how the potential and field lines are drawn and then you will have a field line going from gate to source, something like this. So if you were to extend this equi-potential line, so it will go something like this.

And similarly, here the line would be something like that. You can draw more potential lines between these 2, some of them may go something like this. If you draw a potential line here, it may go something like this and then go up. So that is how your equi-potential and field lines in a MOSFET look like. Now let us show the current flow lines. Now the current will be restricted to the inversion charge here.

To avoid any complication and I do not want to clutter this diagram, therefore, I am showing that separately. So let me show the inversion layer, it will be something like this and the flow lines of the current would therefore be something like this. So the width of the flow here will be more than the width of the flow there. What I have shown is the flow lines corresponding to electrons, okay. So this is where you have your gate.

Now what have we achieved using this equi-potential field and current flow lines. Now we have achieved the following, so we want to highlight the following factors.

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Flow lines for J_n , J_p , E and equi-potential lines for ψ

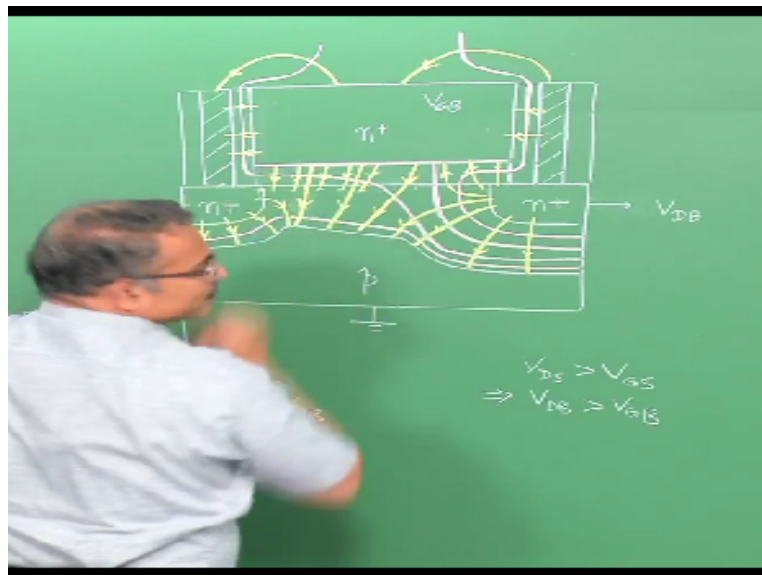
- We sketch the above lines within the oxide, substrate and ambient surrounding the gate, for bias points 1, 2 and 3 to highlight the following:

- 1) A MOSFET, where the current is controlled by a transverse electric field, is inherently a 2D or 3D device, unlike a BJT.
- 2) Field lines from S and D encroach into the channel, reducing the influence of the gate, especially for small L .
- 3) In deep saturation, the reversal of the gate to substrate field complicates the field picture near the drain, making it difficult to derive a physical Channel Length Modulation model.

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First a MOSFET where the current is controlled by a transfer electric field is inherently a 2D or 3D device unlike a BJT. so when you look at this field lines, you can clearly see that they are all 2-dimensional, okay. Now I have not shown the third dimension. If you show the third dimension also, in many cases, the field and potential pictures will be 3-dimensional.

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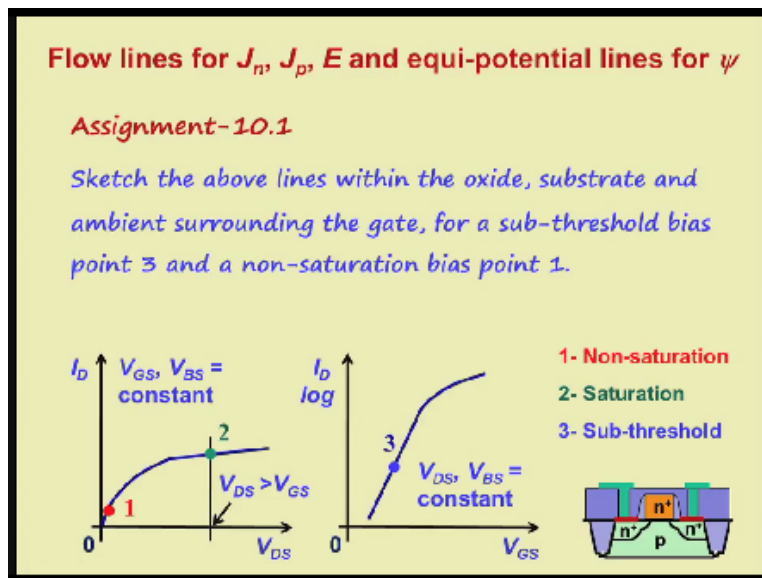
Next field lines from source and drain encroach into the channel reducing the influence of the gate, especially for small L that is small channel length. So you can see here, your field lines are encroaching into this region, okay, you can see there. So I can draw one more line, something like this and similarly, you will have line here. So because the field lines from source and drain

are encroaching into the channel region, the control of the gate over the channel region reduces and if the source to drain distance is small.

Then the control of the channel by source and drain through this field lines will compete with the control of the channel from the gate. Finally, in deep saturation, the reversal of the gate to substrate field complicates the field picture near the drain making it difficult to derive a physical Channel Length Modulation model. So we are talking about this region near the drain where Channel Length Modulation happens.

Here you can see that there is reversal of the electric field while in this region, the field is from gate to substrate. In the remaining part of the channel, it is from substrate to gate. So because of this complicated field picture, physical channel and modulation becomes difficult to derive.

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Towards the end of this lecture, let us give the assignment. Sketch the above lines, that is the flow lines for J_n , J_p , E and equi-potential lines for ψ within the oxide substrate and ambient surrounding the gate for a subthreshold bias point 3 and a non-saturation bias point 1. So this is 3 and this is 1. Now we are not sketching the flow lines for J_p because we have neglected the J_p altogether.

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Summary of the Lecture

With that we have come to the end of the lecture. So let us make a summary of the important points. So in this lecture, we are first explained the behavior of the drain current in subthreshold and breakdown regions. Then we summarized the factors responsible for creation conservation of J_n , J_p and E , that is the creation conservation of current and electric field. Then, we looked at the factors which govern the conditions at the boundaries of the device.

Finally, we have drawn the equi-potential field and current flow lines in the MOSFET to highlight the intricacies of the device physics which govern the current voltage characteristics.