Electronics for Analog Signal Processing - II
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Lecture - 11
Instrumentation Amplifiers

So, we were discussing about these 3 op amp instrumentation amplifiers in the last class and we had gone to the extent of finding out what the common mode gain is from this point to this point and what the differential mode gain is from this point to this point.

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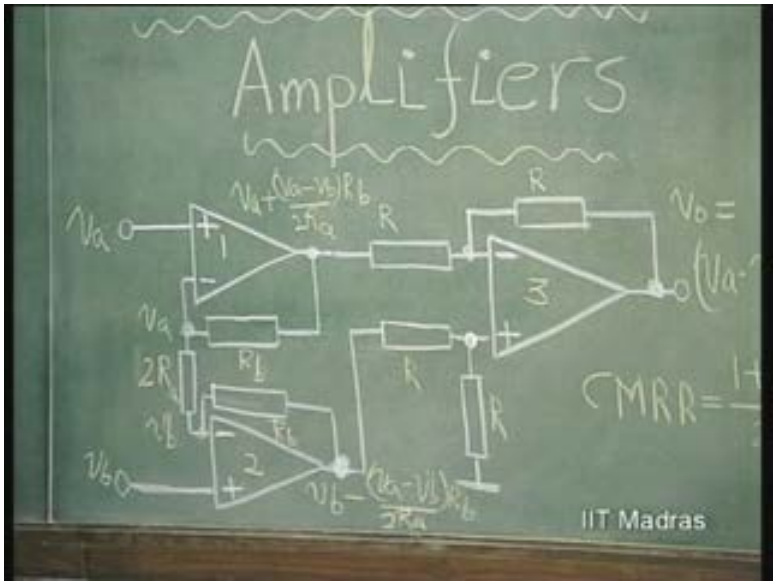

Common mode gain here, common mode voltage here, at the input is V a plus V b by 2. That is the common mode voltage at the input of these 2 amplifiers stage. At the output, again, V c i, V c o, here is again this; also equal to V a plus V b by 2 because these 2 get cancelled. So, the common mode voltage remains same. Gain is 1.

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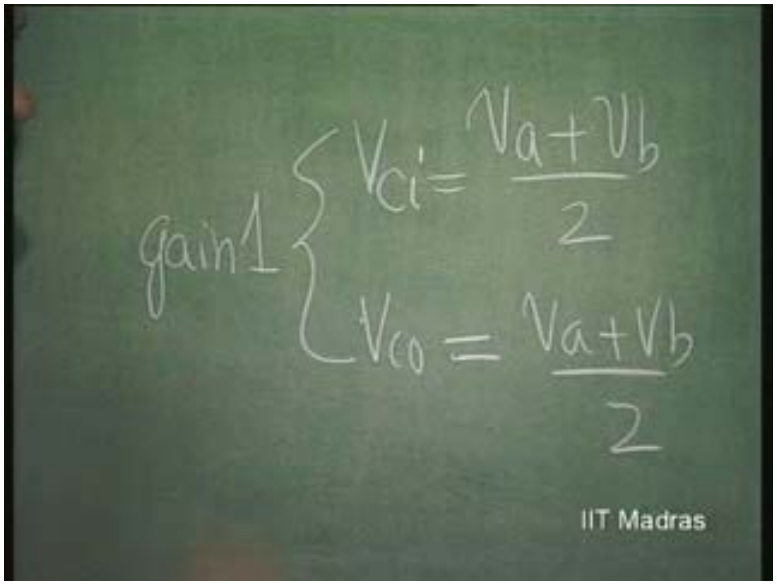

By introducing this stage, as far as the common mode voltage is concerned, the gain is just remaining 1. The common mode voltage input is V a plus V b by 2. Here also, it is V a plus V b by 2. But, as far as differential mode is concerned, here it is V a minus V b at the input; and here it is V a minus V b plus V a minus V b into 2 R b by 2 R a. These two will get added when we subtract it. So, this is equal to V a minus V b into 1 plus R b by R a.

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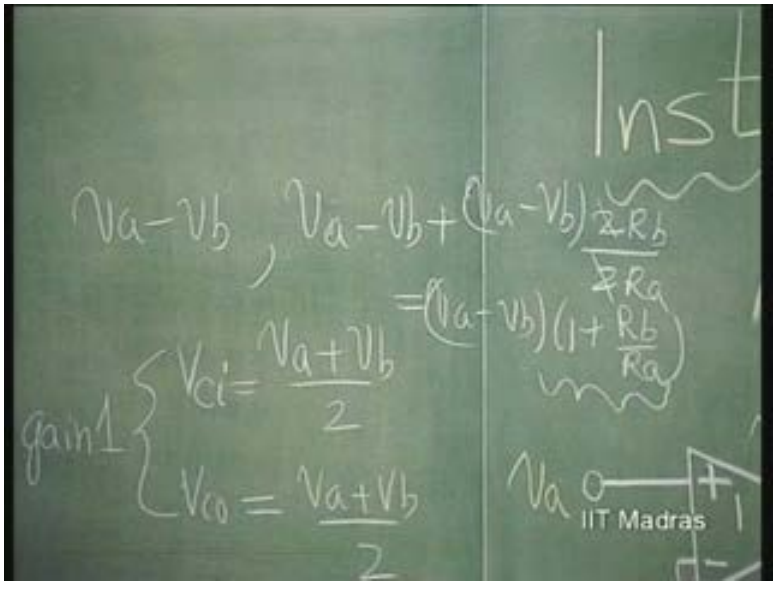

So, we can see that this stage, introduction of this stage of two amplifier has resulted in no change in common mode gain, but an increase in common mode...differential mode gain of 1 plus R b by R a. So, R b by R a can be arbitrarily made high so as to make the differential mode gain very high. And, as far as this stage is concerned, you know that the differential mode gain is 1 because R, R, R, R is chosen and common mode gain depends upon how best these are matched. So, if the tolerance is Delta, that is the tolerance; then, we know that the common mode gain from here to here is going to be 2 Delta; and effect, the differential mode gain of the overall stages, V a minus V b into 1 plus R b by R a and common mode gain is 2 Delta. And therefore, common mode rejection ratio is 1 plus R b by R a divided by 2 Delta.

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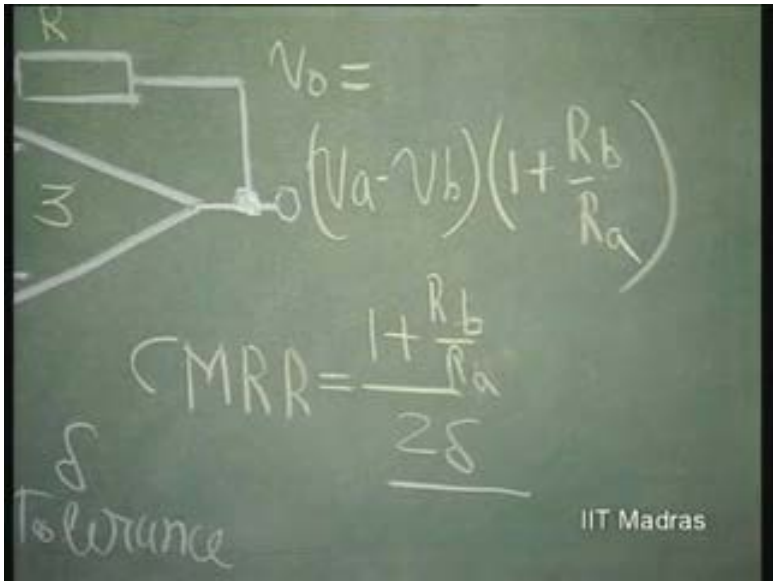

So, this circuit is one of the most popular circuits. It is available as an integrated circuit itself wherein two terminals have been brought out here so that this can be made variable if you want so as to vary the differential mode gain; and you can design it for any differential mode gain that you want. So, this circuit is one of the instrumentation amplifier set up.

Now, another instrumentation amplifier which uses only 2 amplifiers; one and two is shown here.

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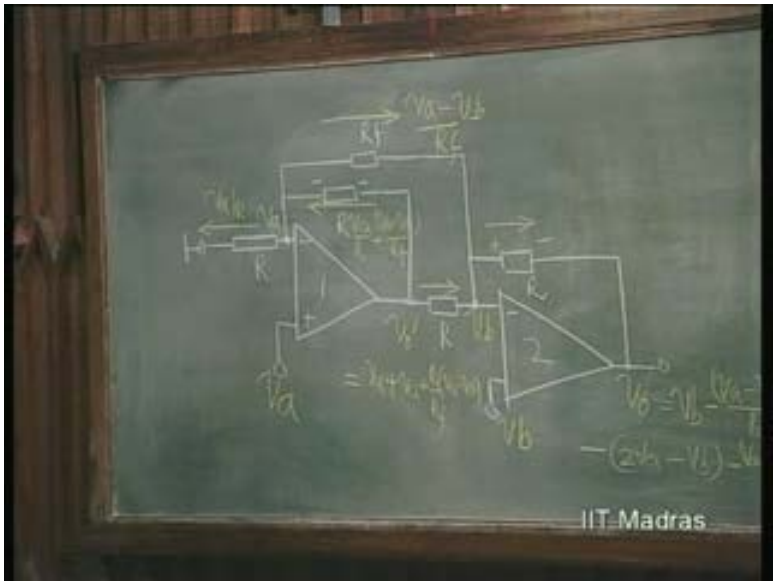

V a is applied here. V b is applied here. And therefore, this voltage is V a and this voltage is V b. So, since this is V a and this is V b, the current in this is V a minus V b by R f. The current in this is V a by R. So, the total current in this is going to be this current plus this current, which is V a by R plus V a minus V b by R f. That is the total current in this.

So, V naught prime here is going to be V a plus the voltage drop across this; which is, this current into R; which is V a plus V a. That is 2 V a, plus R by R f into V a minus V b; that is the voltage at V naught prime. This is V b. This current that is coming is V a minus V b by R f. So, because of this current here, this current plus this current is going to pass through this in this manner; and therefore, the voltage across this is going to be, what is going to be subtracted from V b.

So, V naught is equal V b minus, one current we will take; V a minus V b by R f. That into R. So, minus V a minus V b into R by R f. That is this part of current going through this generating voltage. Then, this current which is twice V a, twice V a minus V b by R

into R. So, twice V a minus V b, one potential; and R by R f V a minus V b divided by R multiplied by R. So, that minus V a minus V b R by R. So essentially, we will see that V naught is going to be equal to this V b; this V b. Twice V b minus twice V a; twice V b minus twice V a; like this. Then, plus V a minus V b into R by R f, V a minus V b R by R f, which is, plus V b minus V a into R by R f 2 times; V b minus V a... So, I can make this plus V b, this is plus, plus V b, minus V a. This can be plus. So, it is V b minus V a by R f into R, twice that.

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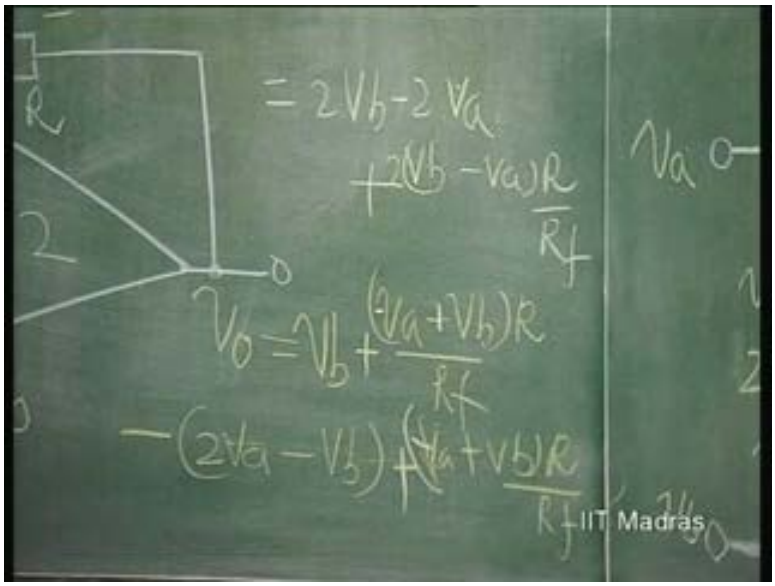

So essentially again, gain is 2 times V b minus V a into 1 plus R over R f.

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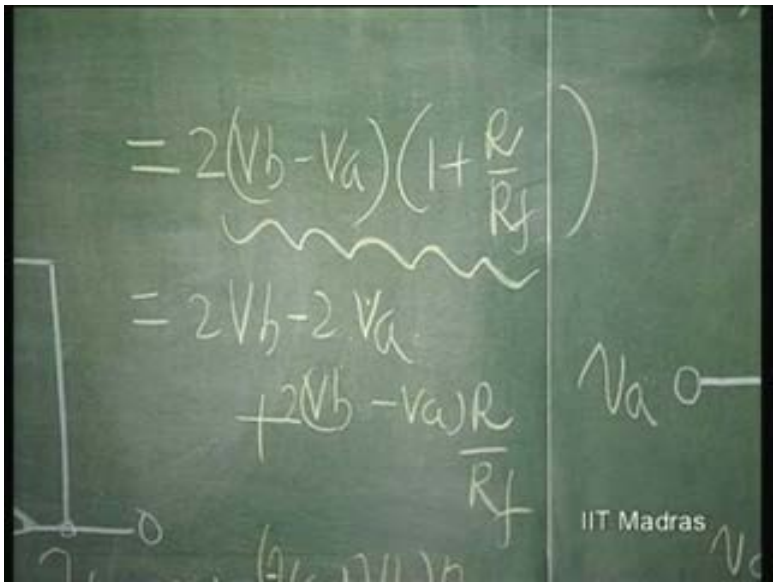

So, once again, we see that this is going to act as a differential amplifier, but uses only 2 op amps; and buffer stage...buffering action is still there because these are the non-inverting terminals here to which inputs are get...fed. So, these 2 instrumentation amplifier configurations are quite popularly used in practice.

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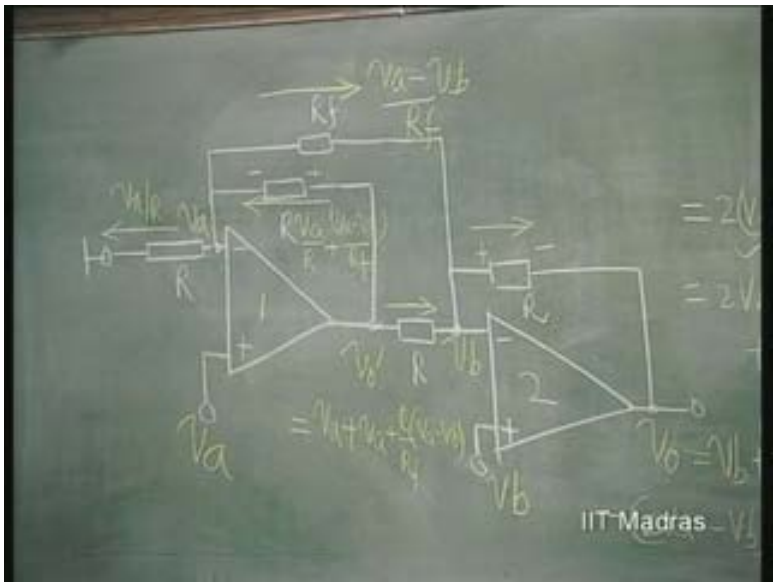

We had discussed how to multiply a voltage by a constant, so far. That is, amplifiers. Then, we have also discussed how we can add voltages and then subtract voltages in the instrumentation amplifier. The other mathematical operations, linear mathematical operations are the following: integration and differentiation.

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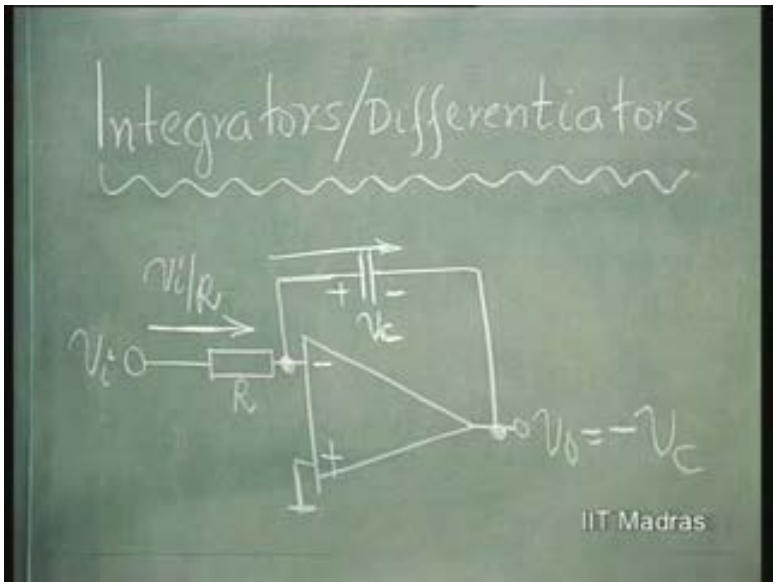

So, let us consider first, how integration is done or differentiation is done. Basically, operational amplifier is going to be primarily used to convert voltage to current. What is done is...integration or differentiation can be done by using a capacitor or an inductor.

We know that if we use a capacitor and an I flow, current I flows through it, through a capacitor of C, the voltage across the capacitor, V, is nothing but 1 over C integral i d t. That is, this is the charge; that divided by capacitor is the voltage across the capacitor. So, this is the basic principal that is used in integration.

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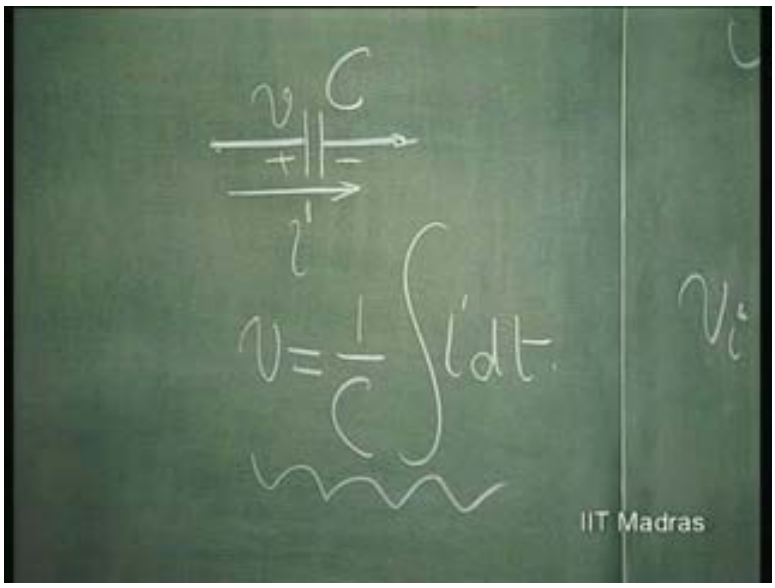

In fact, you can use this the other way about. C d v by d t is equal to I. So, it can be used either as an integrator, or integrator, or as a differentiator. The same capacitor can be used. How do we do it?

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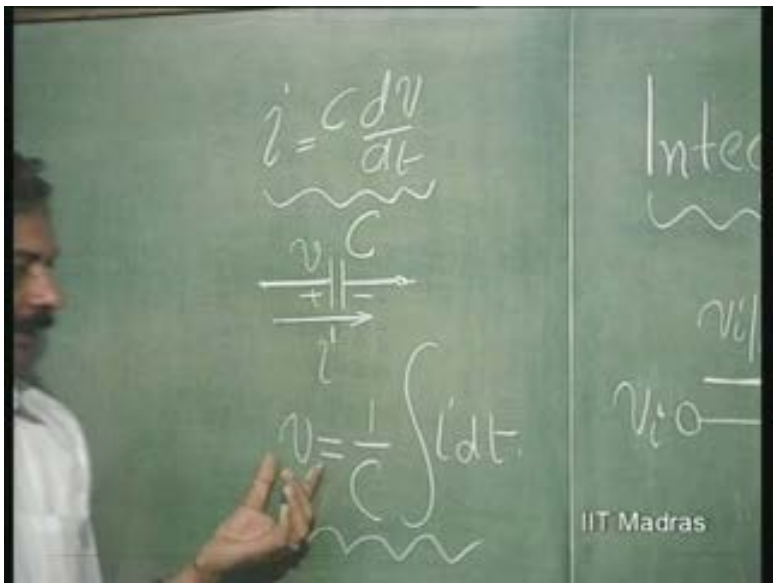

Here, I want a voltage as an integral of another voltage. So, I merely pump into the capacitor a current which is proportional to voltage. So, this facilitates, this op amp here

facilitates, pumping in current because there is a feedback here. This is going to be virtual ground and the current pumped in is V i by R. So, i through the capacitor is nothing but V i by R. So, what happens to the voltage across the capacitor V c? - is 1 over C integral, i through the capacitor, which is, V i by R d t. So, this is nothing but 1 over C R integral V i d t.

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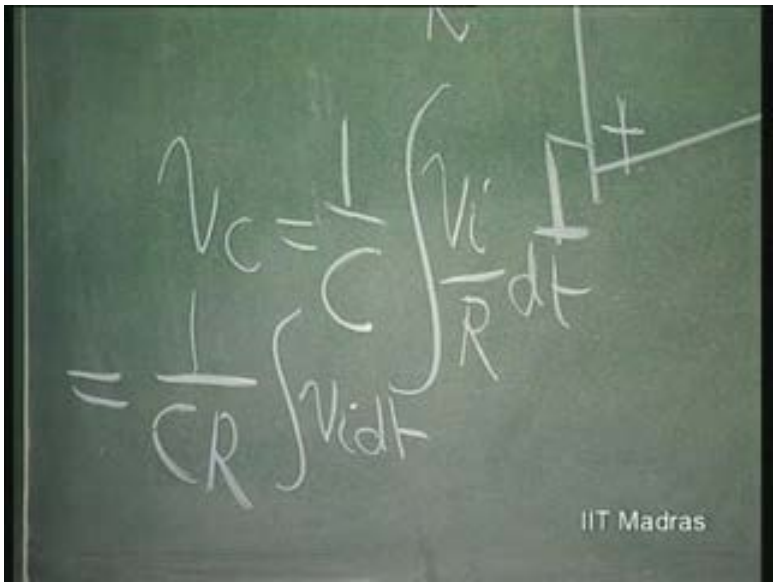

So, I have achieved integration of a voltage and what is V naught? V naught is nothing but minus V c. So, this is minus 1 over C R integral V i d t.

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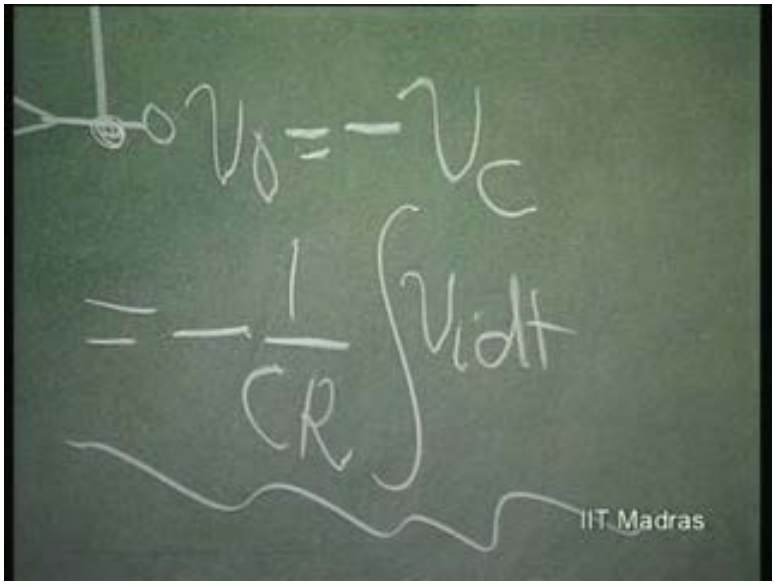

This is an important function, linear function, which is useful for a variety of applications in analog signal processing, integration. How we do differentiation? That is very simple. Once again, we have i equal to C d v by d t. That means, I have to establish a current which is proportional to an input voltage, let us say.

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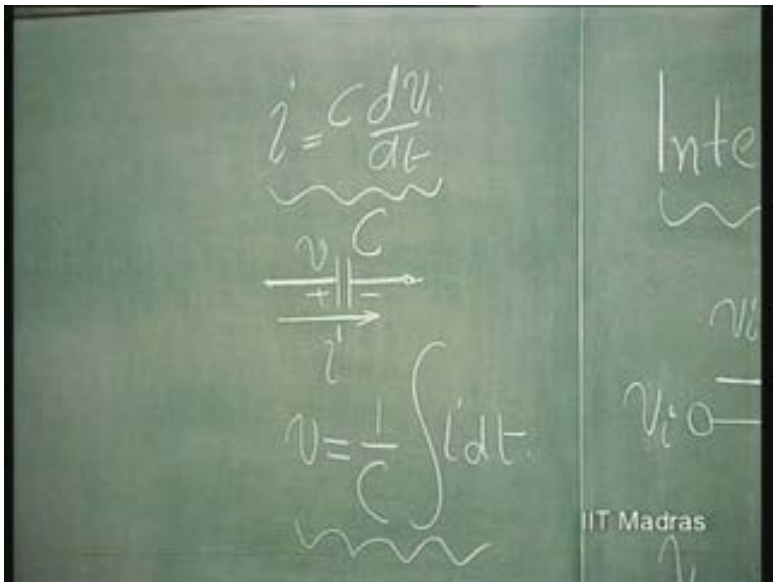

So, I apply the voltage directly across the capacitor. So, V i is applied. So, the current through the capacitor is... this is C... C d V i by d t; according to this, this is the current through the capacitor and the same current is forced to flow through this resistance R and develop the voltage here which is V naught, which is minus this i times... this is I; or this is minus R C d V i by d t.

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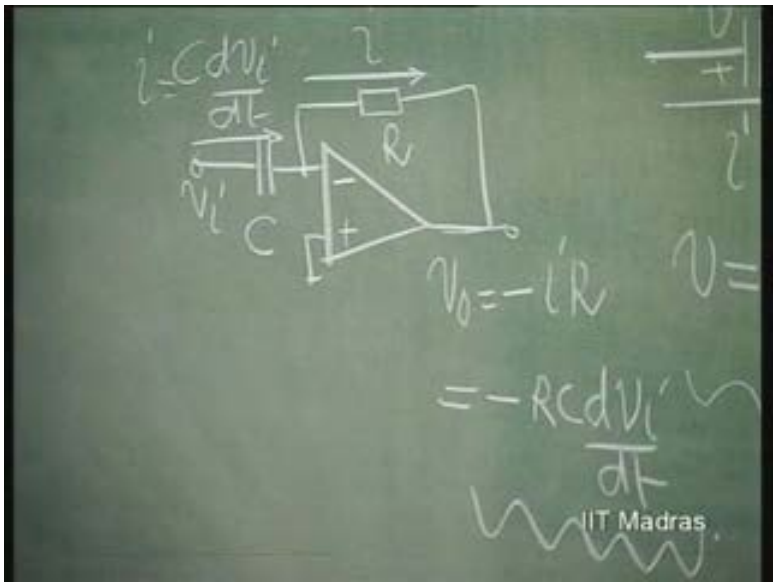

So, straightaway, by interchanging the resistor and the capacitor in this configuration which is inverting, I can achieve integration as well as differentiation. Now, what does it really mean in terms of transfer function? This also can be done. We can replace this - instead of the time analysis, by the frequency analysis, here. So, the impedance of this is 1 over S C and therefore the same thing is valid here.

We have V i naught, the R M S value of the input voltage, and the current is V i by R. That remains the same. The voltage here therefore, is going to be V i by R minus V i by R into 1 over S C. The transfer function V naught over V i is minus 1 over S C R. 1 over S means integration.

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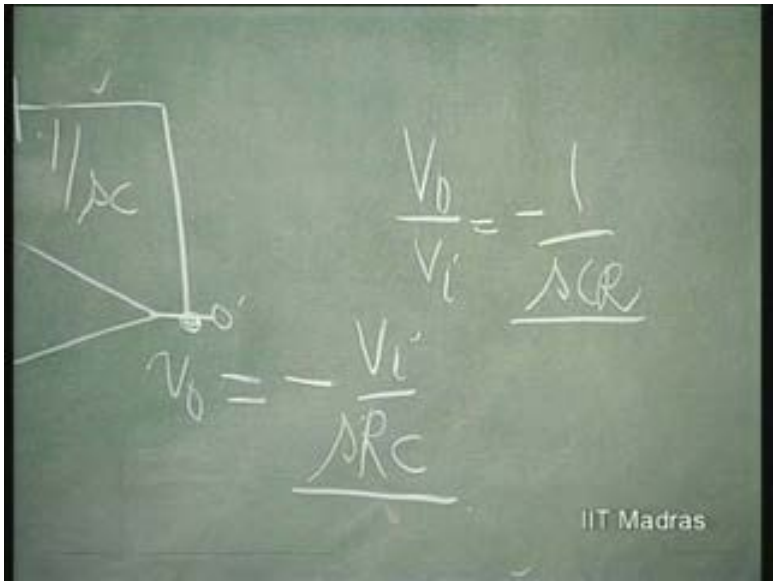

Similarly, it can be shown that d V i by d t means, yes, differentiation. So, this is equal to V naught over V i equal to minus S C R.

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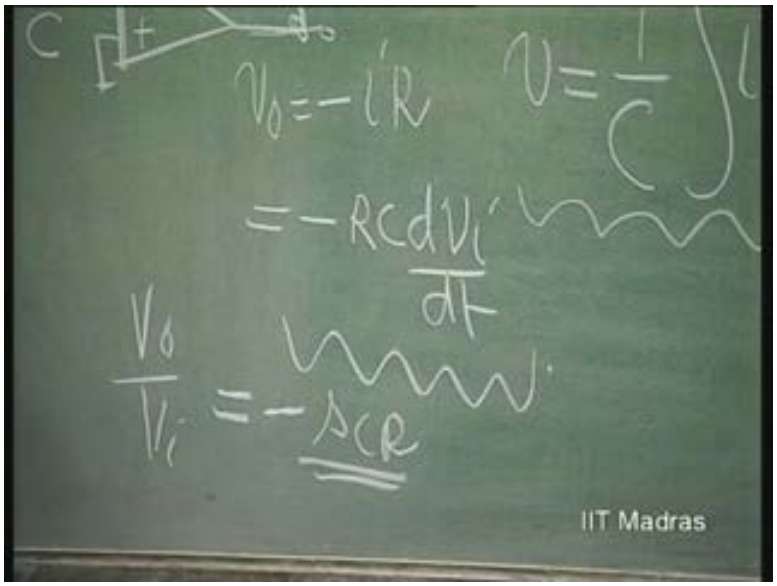

Again, we can replace this by V i. This by 1 over S C and the current is going to be S C into V i. That is the current through this capacitor and the potential here is going to be S C V i into R with a negative sign. So, S C R here.

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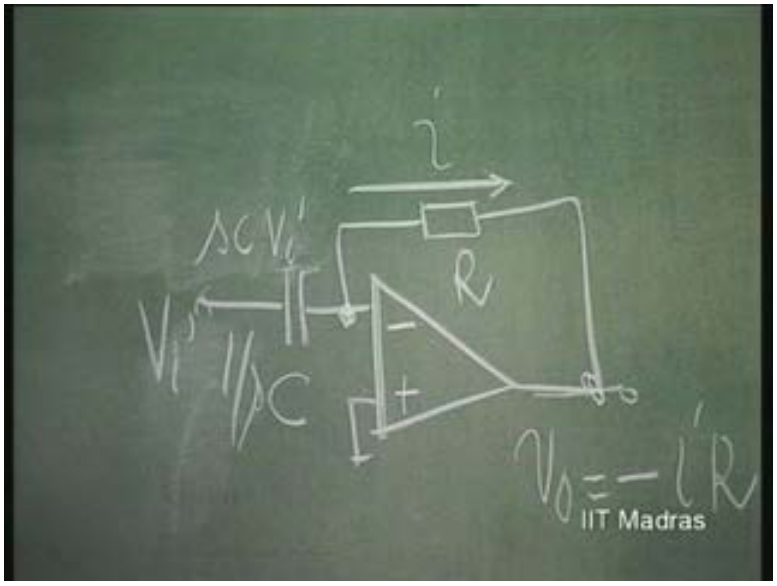

So, these are the transfer functions of these 2 blocks which are very important linear building blocks. What happens? Let us understand. For D C that is put S equal j Omega and consider for D C; Omega is equal to zero. The gain is infinity.

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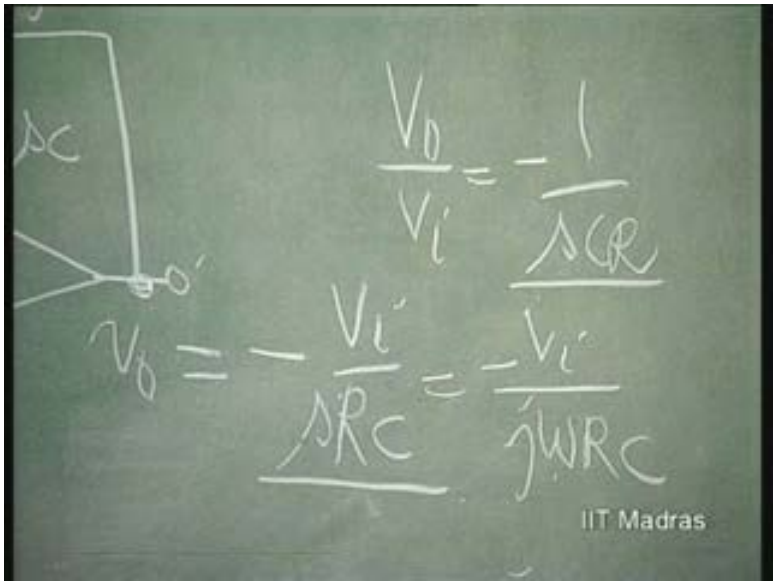

So, for an integrator, if you apply a D C, the gain is infinity; and therefore, ultimately, output will go to saturation. Even if there is a small value of D C voltage here, it will keep on integrating and output will go to saturation.

So, this is something that you have to bear in mind. This integrator, even without any input, may go to saturation simply because of the offset voltages which are of the order of millivolts, which are already there in practice, in the input of an operational amplifier.

So basically, giving an input D C here has this problem with this integrator that it invariably lands up in saturation; whereas in the case of a differentiator, there is no such problem. There is negative feedback as far as D C is concerned and the gain for D C is zero because the capacitor is decoupling the D C. So, gain for D C is zero.

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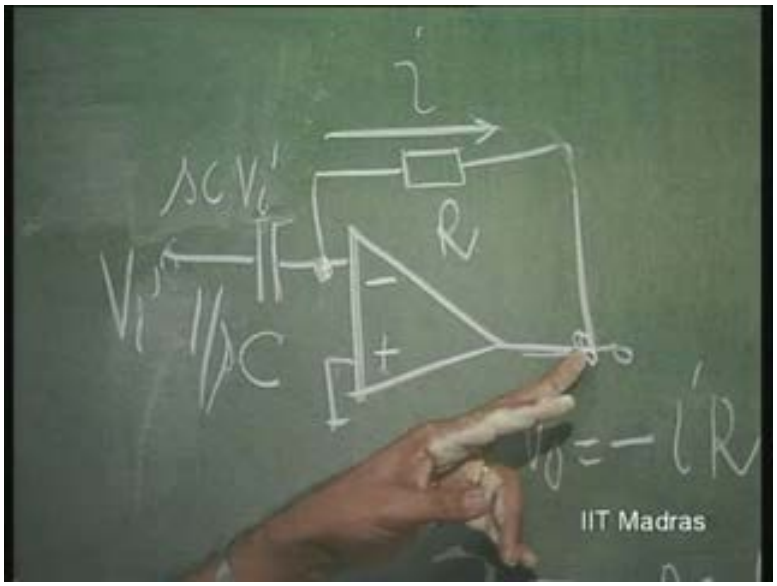

And, as far as this operation is concerned, this is grounded. So, this is at zero volts and output voltage will be stably at zero volts. So, that is the advantage of biasing of the op amp in the case of differentiator as against that of integrator because there is no D C feedback, negative feedback, because of the capacitor. And therefore, biased stabilization

is very difficult to achieve. The offset, input offset, is going to make the output go to saturation.

So, we can also see what happens when I apply a sine wave here. We can see that there is a phase shift of 90 degrees; because of j, there is a phase shift of 90 degrees between the output and input. So, this is the case with differentiator also. There is a phase shift of 90 degrees.

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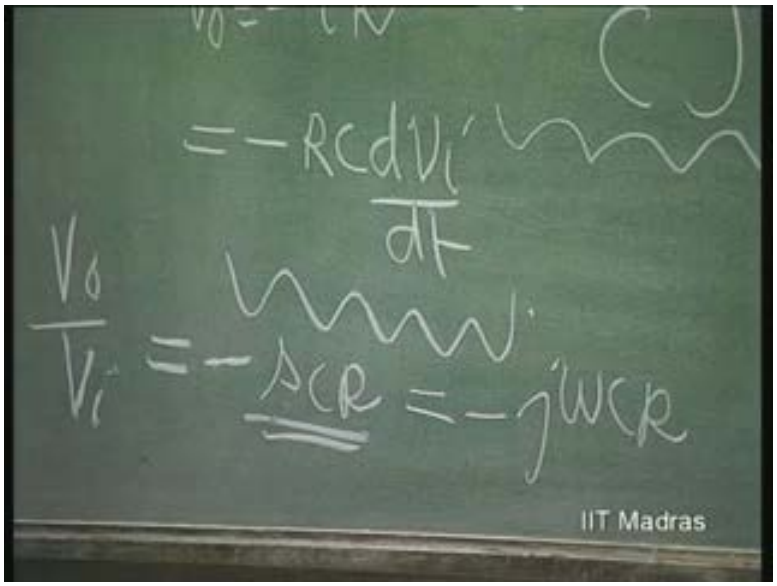

So, both these blocks can be used to obtain an output which is in quadrature with the input; phase shift of 90 degrees means, output is in quadrature with input. That means, if output...input is a sine Omega t, output will be b cos Omega t. So, this quadrature component can be obtained easily by using integrators.

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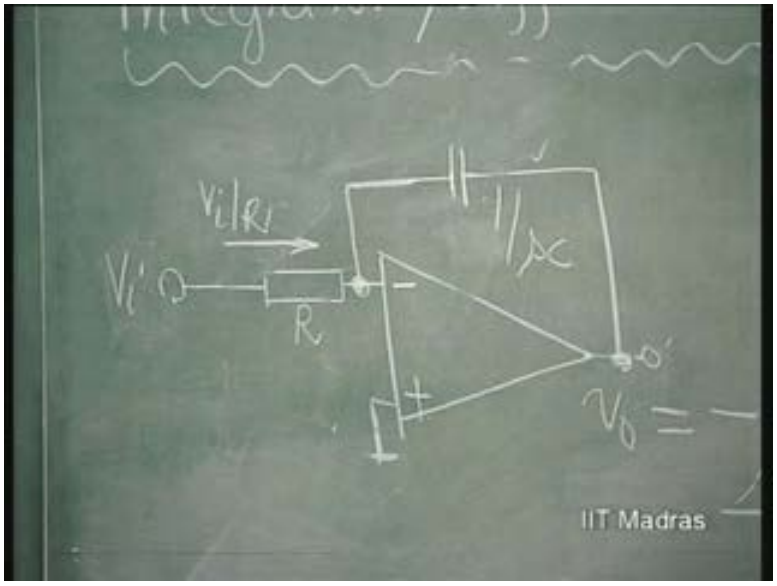

Next, integrator is something whose gain is inversely proportional to frequency. That means at high frequency, it eliminates all the signals; whereas differentiator is something that will amplify all high frequency components. That means a differentiator will respond even to noise which is occurring at high frequency.

That means, if there is a voltage induced because of somebody starting a scooter or car or anything that will disturb this differentiator, because that will appear at the input as an induced voltage and that will be amplified considerably by the differentiator. So normally, differentiators like this are not used because they are amenable to noise. They are disturbed by, their output is disturbed by, sudden fluctuation of voltage which can be picked up and that will be amplified at the output considerably; whereas integrators do not have that property because they will suppress the noise at high frequencies.

So, if it is just quadrature component you want, you would rather use an integrator than a differentiator; but the trouble with the integrator is, as such, because of no D C negative feedback, output is liable to drift and go to saturation. So, you might have to really provide D C negative feedback in order to stabilize output. We will see this later - how integrators can still be used with overall D C feedback so as to stabilize the D C at zero.

So, consider Example 7 which is to design a summing amplifier using only one op amp to give an output V naught equal to point 1 V i 1, minus point 7 V i 2, plus 100 V i 3, minus 10 V i 4. So, these have been arbitrarily chosen so as to facilitate design of any generalized summing amplifier. Co-efficients can be less than 1 or greater than 1; can be positive or negative.

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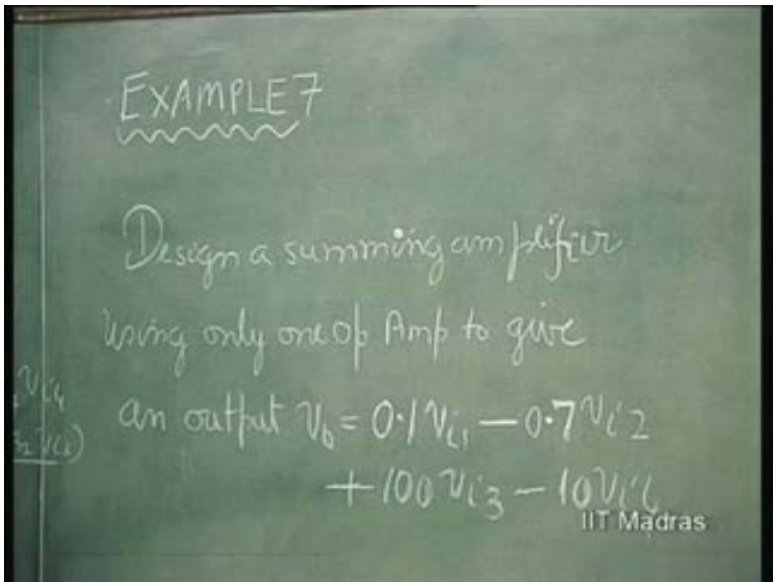

So, how to now approach this problem of designing using only one op amp. A generalized summing amplifier so that the design is strictly over. Now, let us concentrate on this op amp now.

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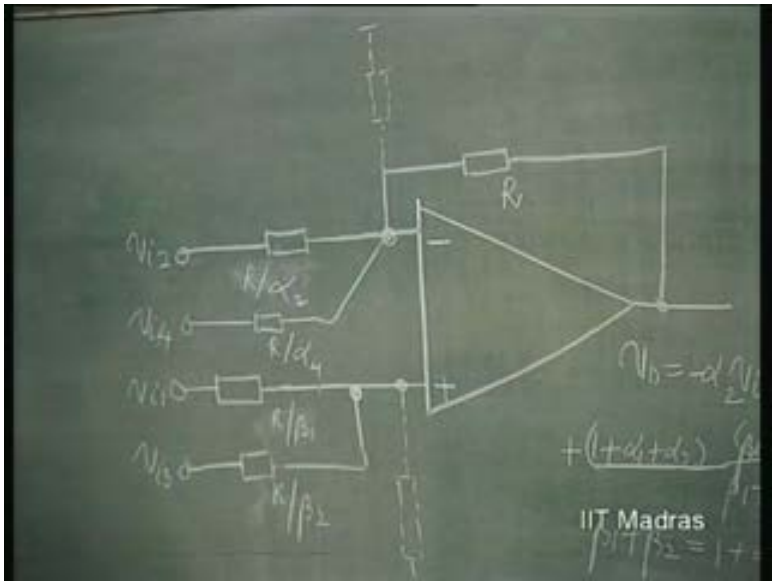

We are giving negative feedback here and as I told you, with negative co-efficients like in this case, minus point 7 and minus 10, can be easily got by designing an inverting amplifier. So, V i 2 and V i 4 which have negative co-efficients can be fed to the op amp through resistors which will come to this point, so that these inputs, irrespective of the inputs connected to positive...when these inputs are not considered, these can be connected to ground. So, this will be ground potential and this will be virtual ground, we said; and therefore, all these currents are going to get added.

So, V i 1 divided by R by Alpha 2 which is V i 1 V i 2 into Alpha 2; divided by R multiplied by R. So basically, you get minus V i 2 here, which is this resistance divided by this resistance is the gain, with the inversion sign. So, R divided by R by Alpha 2. So, the co-efficient is neatly chosen as Alpha 2.

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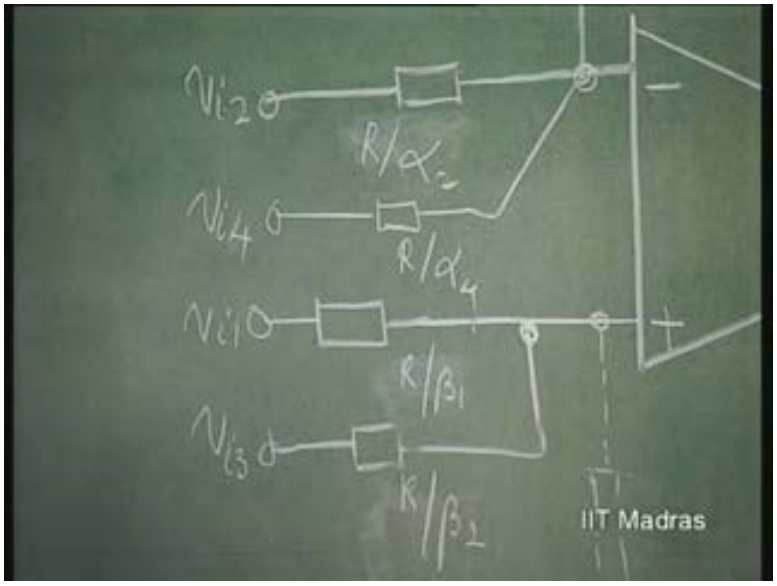

So, Alpha 2 in this case happens to be, let us say point 7. So, Alpha 2 therefore is point 7, easily identified. So, this is over.

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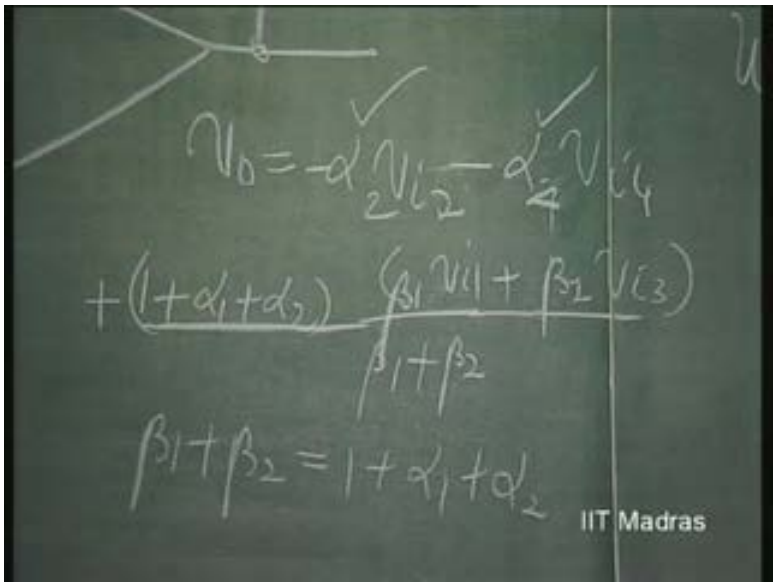

Then, it will also sum up this V i 4 divided by R by Alpha 4 which is V i 4 into Alpha 4, divided by R, multiplied by R, develops a potential which is minus Alpha 4 V i 4. That we know. This divided by this resistance is the gain with an inversion sign, Alpha 4.

So, Alpha 4 is going to be equal to, according to our requirement is 10. So, very simple design. So, we have chosen Alpha 4 as 10. So, if this is 1 K, this is going to be 10 K, this is going to be point 7 K. That is... sorry. This is going to be... if this is 1 K, this is going to be 100 ohms because R by Alpha 4, 100 ohms. This is going to be 1 K by point 7. Therefore, we have easily chosen these co-efficients in this manner. Now, coming to to this... So, this is also finished.

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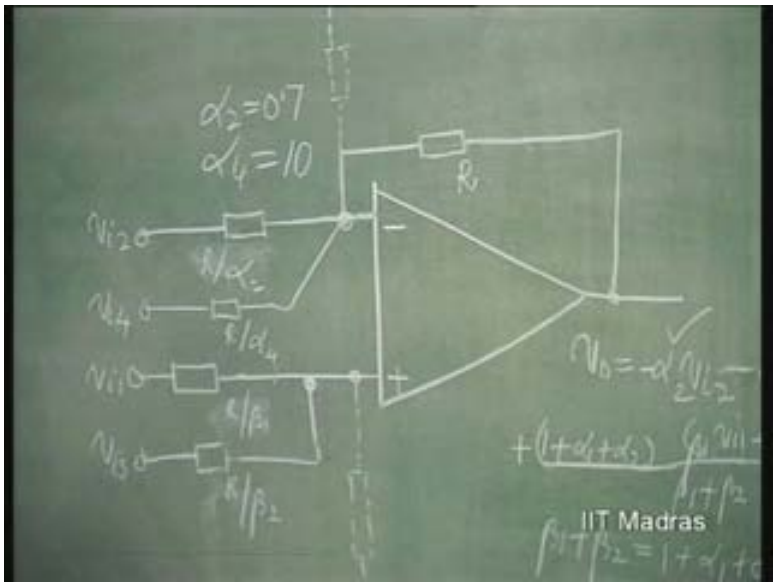

What happens now to inputs which are connected here? These inputs will be amplified without any phase shifts or they do not have any change of sign. These are fed to the non-inverting terminals. So, from here to here, there is a gain. You assume that these are grounded here now because we already considered what the output is due to this. So, these are not going to be disturbed. In addition, we will have an output due to this which is coming here. The voltage that is coming here because of this V i 1 and V i 3, which both have positive co-efficients, V i 1 and V i 3. This has point 1, this has 100. This voltage is appearing here. So, in order to adjust that co-efficients, I am putting some resistances through this.

This is R by Beta 1; this is R by Beta 2. Suppose I put this. Then what is the resultant voltage here? This will be from here to here. It will act as a non-inverting amplifier because you have 2 resistances coming in parallel here and there is a resistance in the feedback.

So, this is your effective R 1; this is your R 2. That means gain is 1 plus R 2 over R 1, which will be 1 plus Alpha 1 plus Alpha 2. So, the gain from here to here is going to be this - 1 plus Alpha 1 plus Alpha 2. Why? If this whole combination is R 1 and this is R 2, R 2 is equal to R. The gain we have known is 1 plus R 2 over R 1.

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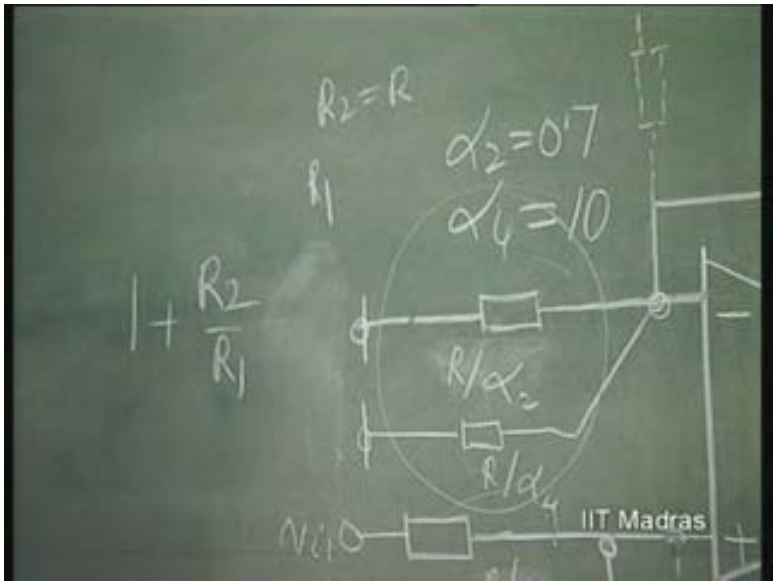

That means 1 plus R... R 1 is parallel combination of this, which is, Alpha 2 over R plus Alpha 4 over R. So essentially, you will get the gain as 1 plus Alpha 1 plus Alpha 2. Alpha 4; sorry.

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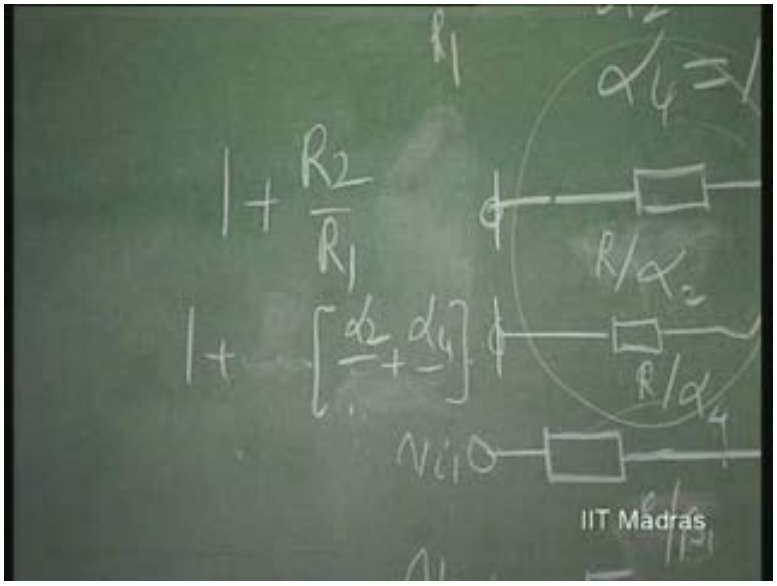

Then, the attenuation because of this is Beta 1 divided by Beta 1 plus Beta 2. Actually speaking, it will be this resistance divided by this plus this for this; this resistance divided by this plus this.

So, for example, for V i 1, it will be R by Beta 2 divided by R by Beta 1 plus R by Beta 2, which is really Beta 1 divided by Beta 1 plus Beta 2 times V i one. That is all. Beta 1 by Beta 1 plus Beta 2.

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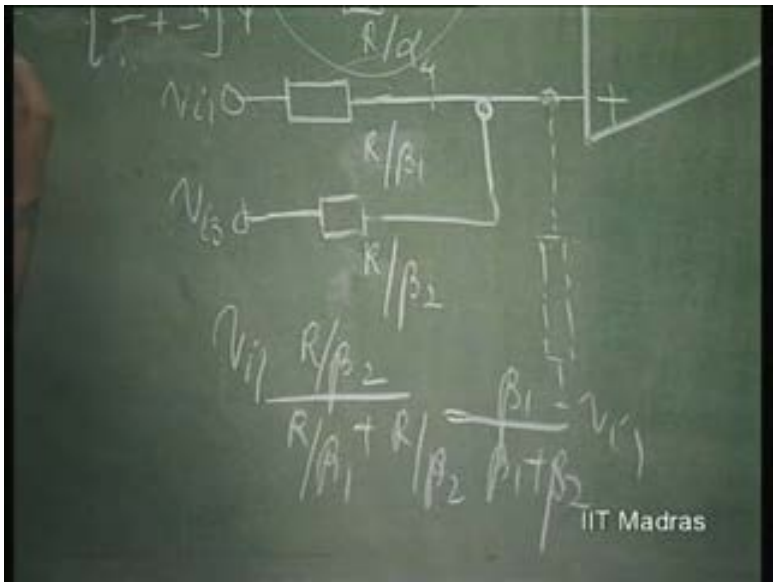

The other one is Beta 2 by Beta 1 plus Beta 2. Easy way to remember this is, if this is a conductance which is Beta 1 into g, if this is a conductance which is Beta 2 into g, it is that conductance which is connected to that voltage divided by sum of all conductances. So, Beta 1 g divided by Beta 1 g plus Beta 2 g. This voltage is Beta 2 g divided by Beta 2 g plus Beta 1 g. That is all.

So, that is the... And if I make Beta 1 plus Beta 2 equals 1 plus Alpha 1 plus Alpha 2, this I have to see.

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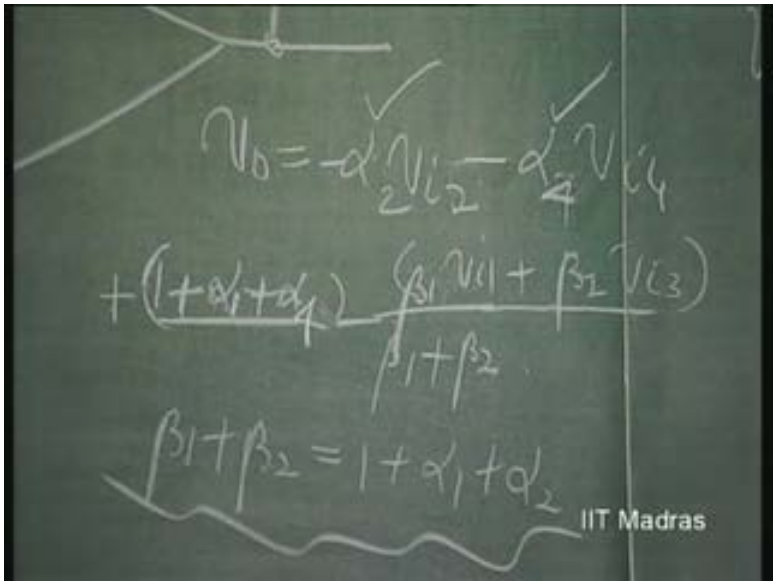

Then, I can conveniently select Beta 1 as V i 1 coefficient which is point 1 and Beta 2 as V i 3 co-efficient which is 100; so, this kind of design, can I do?

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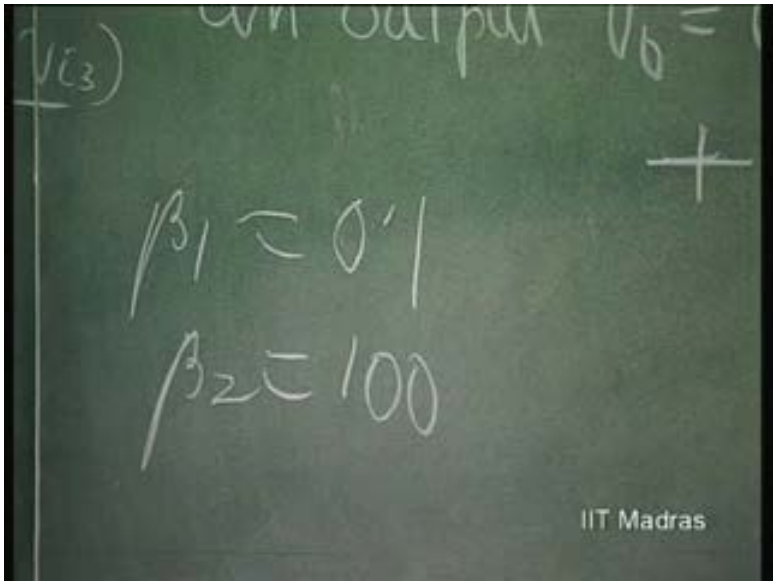

I have to have now Beta 1 plus Beta 2 equals 1 plus Alpha 1 plus Alpha 2. Therefore, I can cancel this. How do I do this? Now, let us see in our design.

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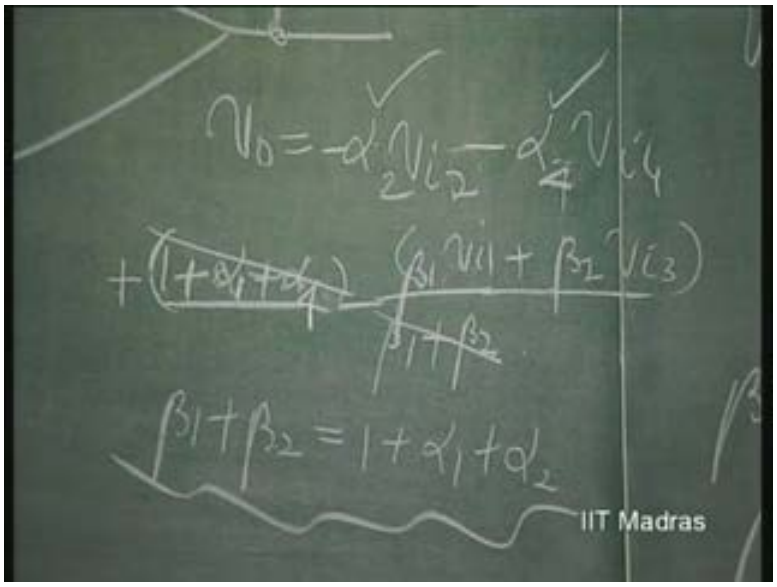

1 plus Alpha 2 plus Alpha 4 is this; 10, 11, equal to 11 point 7. That is 1 plus Alpha 2 plus Alpha 4.

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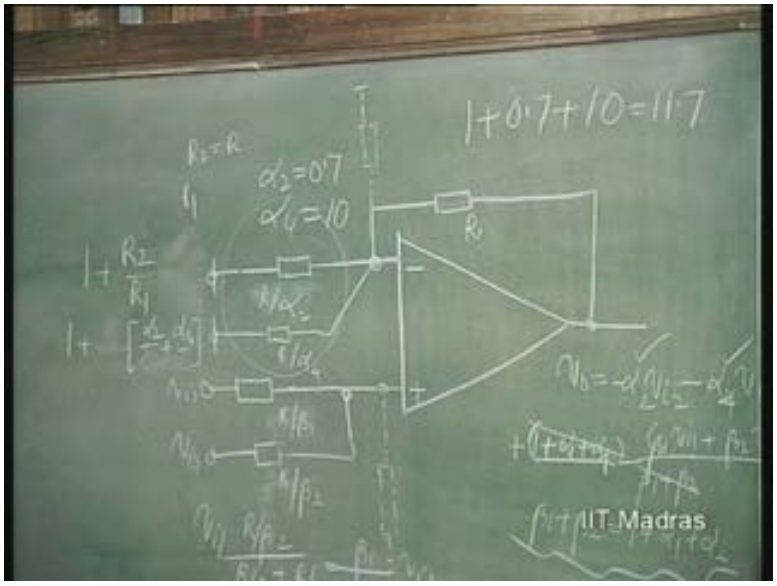

Beta 1 plus Beta 2 is going to be how much?

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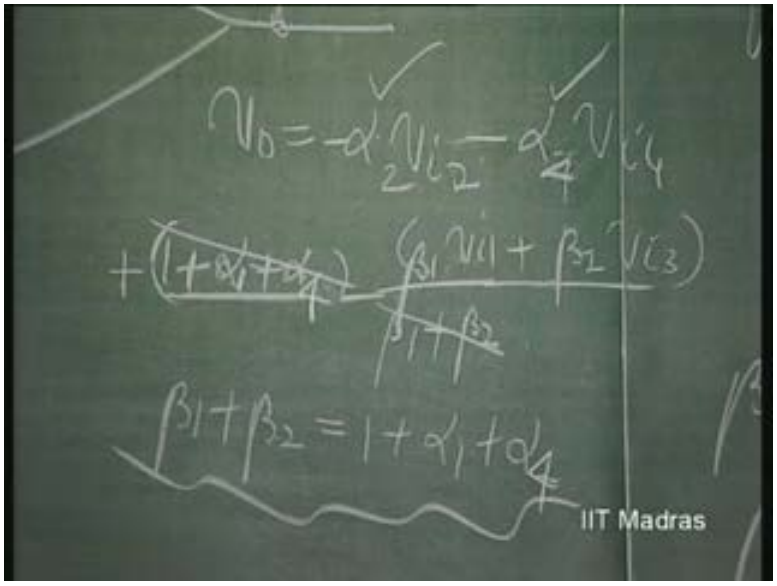

Beta 1 plus Beta 2. This is 1 plus Alpha 1 plus Alpha 4. This is equal to point 1 plus 100. 100 point 1. Which is greater? This is greater. Beta 1 plus Beta 2 is greater than 1 plus Alpha 1 plus Alpha 4 by an extent which is, let us see. That is all. 88 point 4. How do I give this? How do I therefore satisfy this?

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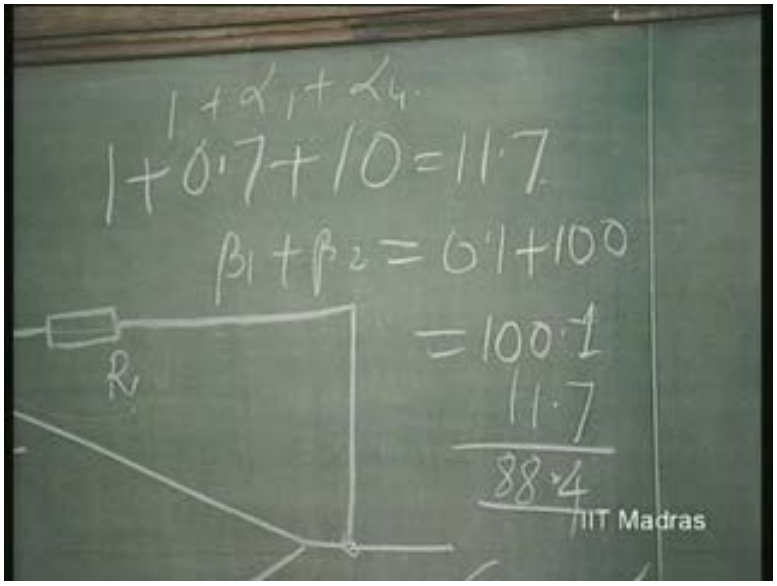

So, I have to introduce something along with this so that this will be, let us say, some Alpha zero which is 88 point 4. Then, this condition will be satisfied.

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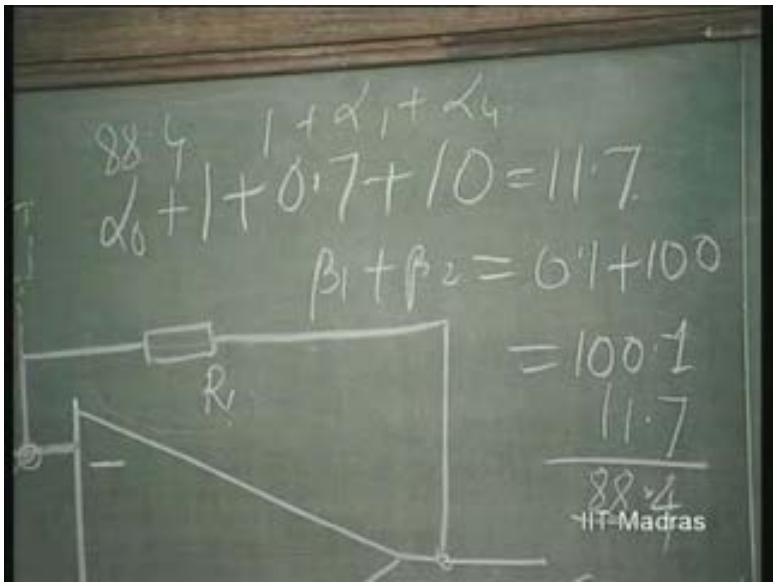

So, I have to introduce here an Alpha zero which is 88 point 4. Then this condition is satisfied. So, but that Alpha zero should not be connected to any input voltage because it should not contribute to any output.

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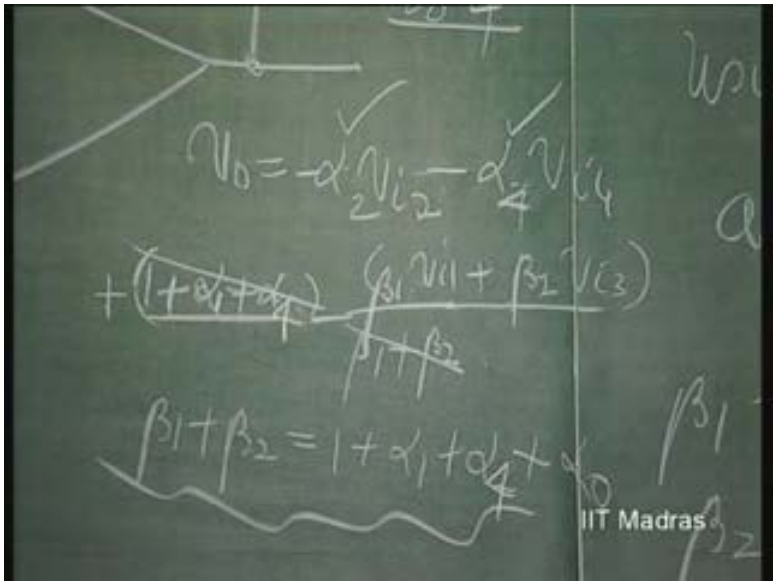

So, I simply put a resistance here with R... the input to this is zero; dummy resistance so that this generates an Alpha which is R by Alpha zero and Alpha zero is equal to 88 point 4. Now, this will have 1 plus Alpha zero; and we have purposely selected Alpha zero so that Beta 1 plus Beta 2 is equal to 1 plus Alpha 1 plus Alpha 2 plus Alpha 4 plus Alpha zero. They get cancelled here and we get this design in a very simple manner representing straightaway... Answer is very simple.

Alpha 2 is corresponding to point 7. Alpha 4 corresponds to 10. Beta 1 corresponds to point 1. Beta 2 corresponds to 100. Then, I have to make only Alpha zero adjustments so that my design becomes very simple. So, whether I use here any number which is greater than 1 or less than 1, positive or negative, these designs will remain very simple in terms of these Alphas and Betas. So, this is the technique of designing it.

Now, one word of caution. It may not be that the resistance, dummy resistance, always comes here to ground. When, for example, here, 1 plus Alpha 1 plus Alpha 4, if it is greater than Beta 1 plus Beta 2, you might have to put a resistance here to ground. So, it is either this to ground or this to ground. That depends upon the relative magnitude of Alphas plus 1 with Betas, added together. So, this is a very intelligent design, actually, so

that, the designer looking at the problem can straightaway write down the answer without much of an exertion on his part.

Historically, operation amplifiers have been used in what are called as analog computers, in simulation of differential equations. Therefore, let us see how the present day op amps also can be used for that purpose. The op amps are available as components and therefore it is very easy to simulate these equations using such operation amplifiers.

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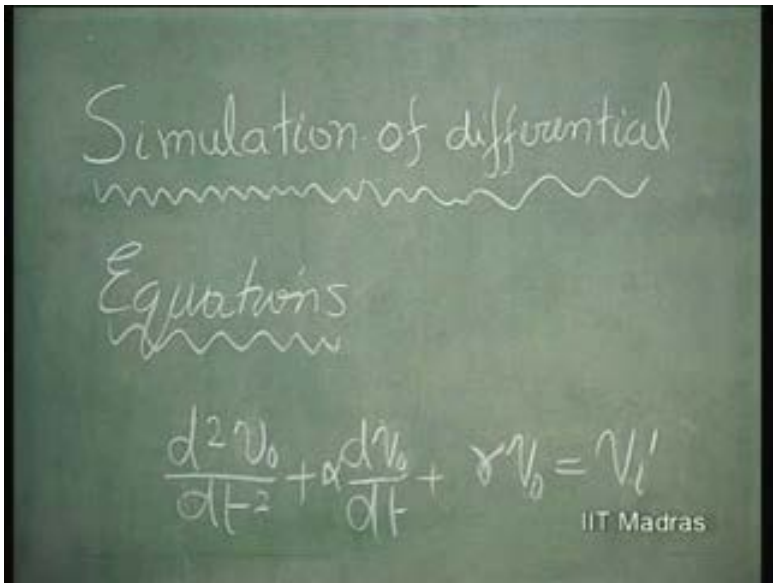

Therefore, the variable I am taking here is voltage. So, d square V naught by d t square plus some Alpha d V naught by d t plus Gamma V naught is equal to V i, is a second order linear differential equation. Second order. This is the order. Second order linear differential equation, I want to simulate.

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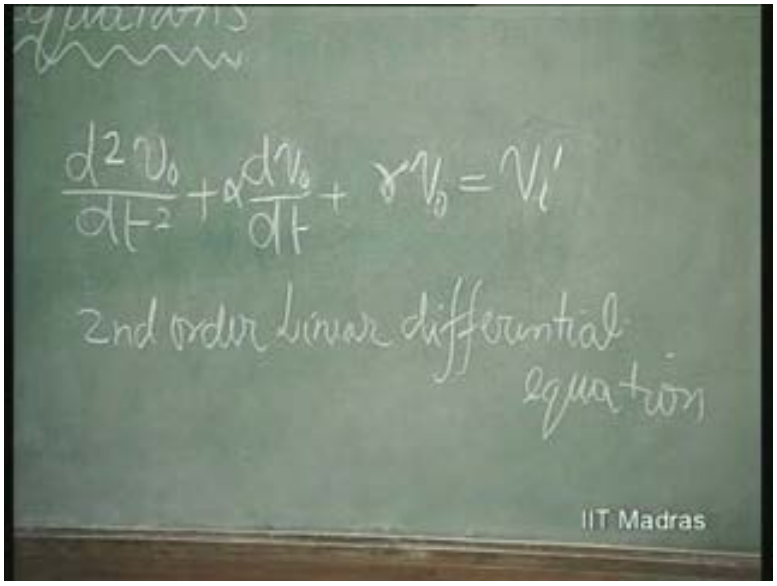

What you do is d square V naught by d t squared equals, from this equation, V i minus Alpha d V naught by d t minus Gamma V naught. The same equation is rewritten this way.

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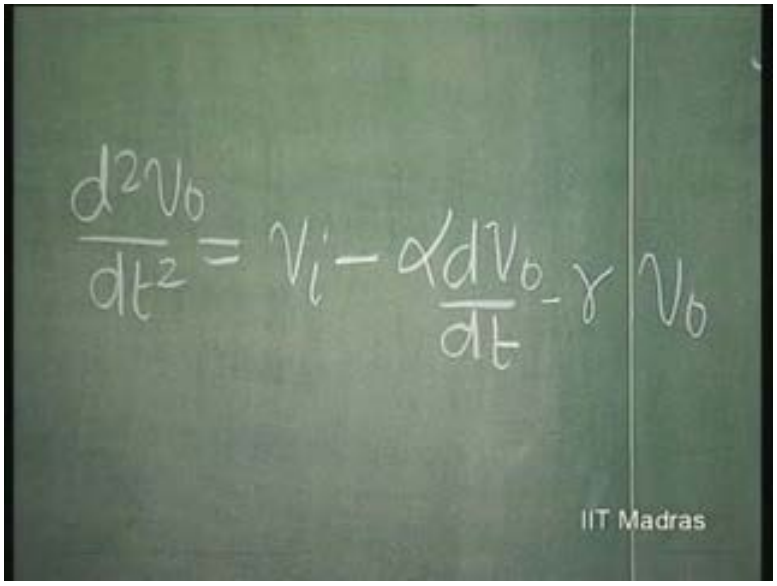

So, what we start with is, let us assume that d squared V naught by d t squared is somehow available to us. Suppose d square V naught by d t square is available to you.

How will you obtain d V naught by d t? You will integrate it once. So, I put an integrator here. This is, I say, R, C. So, output is going to be minus 1 over R C. That is what we have seen earlier. Integral of d squared V naught by d t square which is d v naught by d t.

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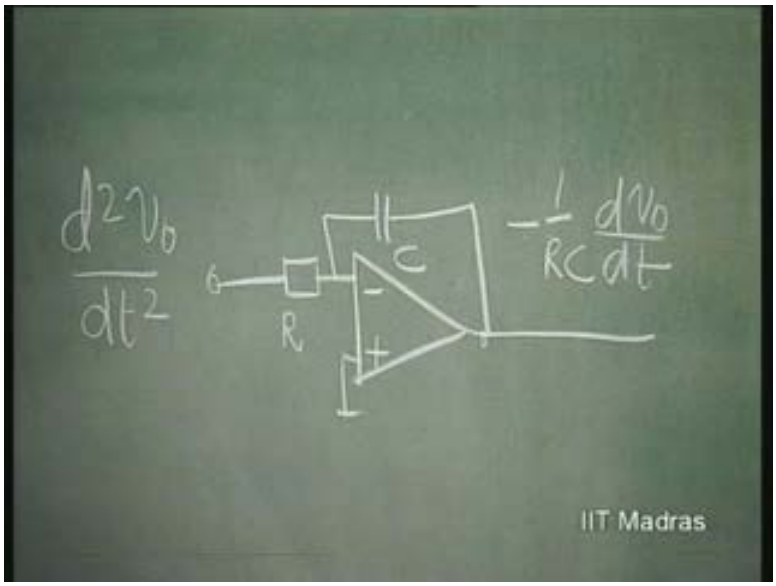

So, you got d V naught by d t by integrating d squared V naught by d t square. Now, using this, if I once again integrate, I can get V naught. So, I put another integrator. So, at the output of this, this is going to be integrated. Again, plus 1 over R square C square because this R C comes into picture. Integration of d V naught by d t and sign becomes plus. So, this is V naught.

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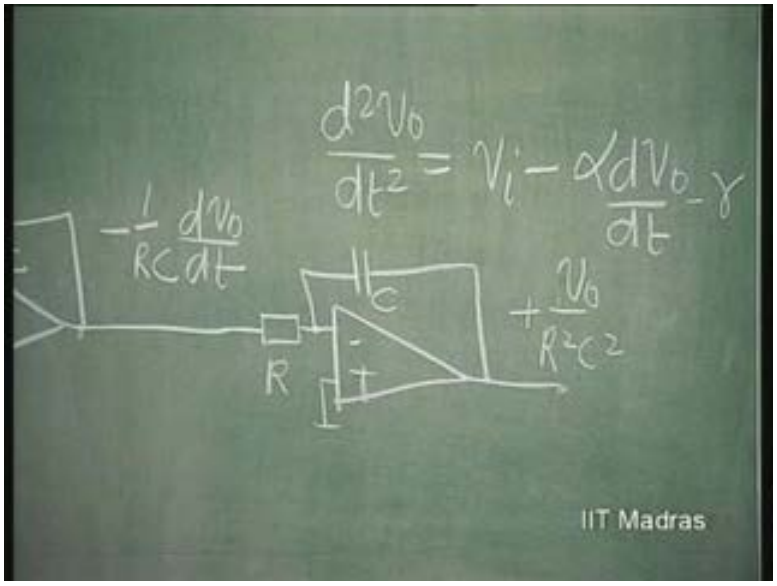

So, I have got V naught with some constant factor, d V naught by d t with some constant factor and a negative sign. So these 2 things are created by me assuming that d squared V naught by d t squared is available. V i can be happily added. V i is an independent input. So, V i is available, this is available, this is available. How do you get, therefore, summation of all these things? Let us see. V i should be added without any, let us say, inversion or anything. Fine.

V i is to be connected to the non-inverting terminal because co-efficient of V i is positive. Let us see another thing. As far as this d V naught by d t is concerned, already there is a negative sign and that has to come as such, without any change of sign. That means this also should be connected to the non-inverting terminal.

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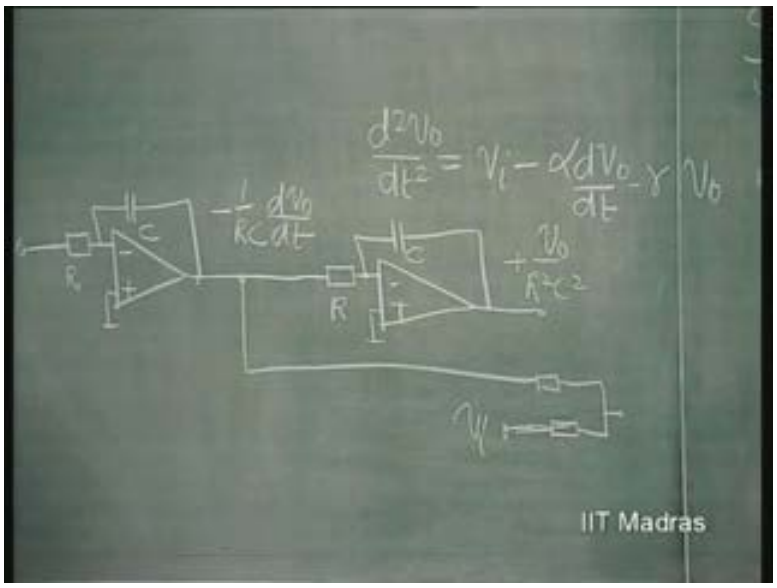

So, what I do is I put here Alpha R and 1 minus Alpha R. So, what happens here?

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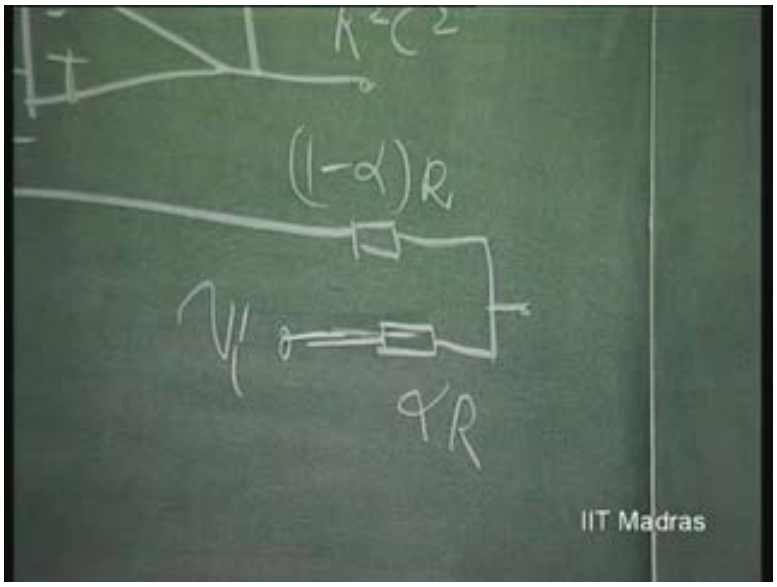

This output will come as Alpha times... let us call it Alpha zero, in order for this thing to... Alpha zero times this value, of which will come here. Alpha zero times minus 1 over R C d V naught by d t will come here, because of this attenuator. And what other portion of V i will come here? Plus V i into 1 minus Alpha zero.

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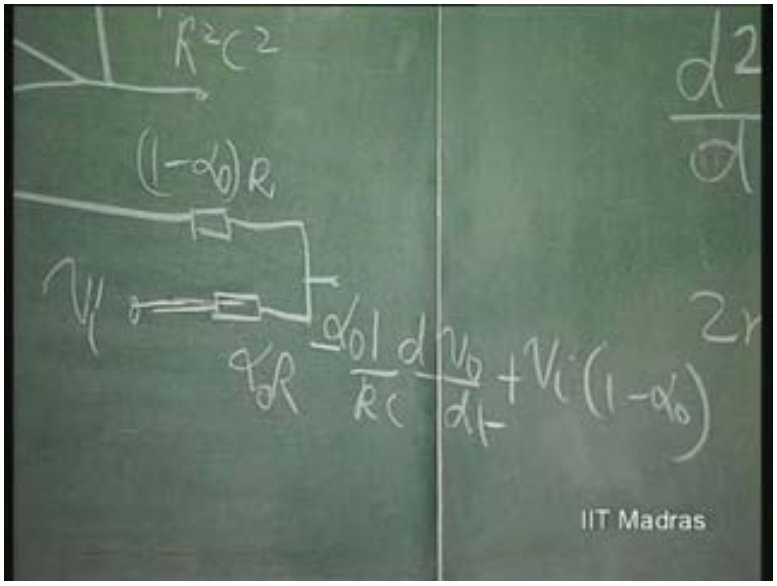

By putting this attenuator, I have got this part as well as this part with some other co-efficients here. We can change the co-efficient by again, using some other multiplying factor while adding.

And then, this V naught by R square C square is positive. But I want a negative sign. So, this has to be applied to the inverting terminal of this summing amplifier. This we have already discussed earlier. How to design the summing amplifier.

So, I can now change this sign here by using, let us say, R and R.

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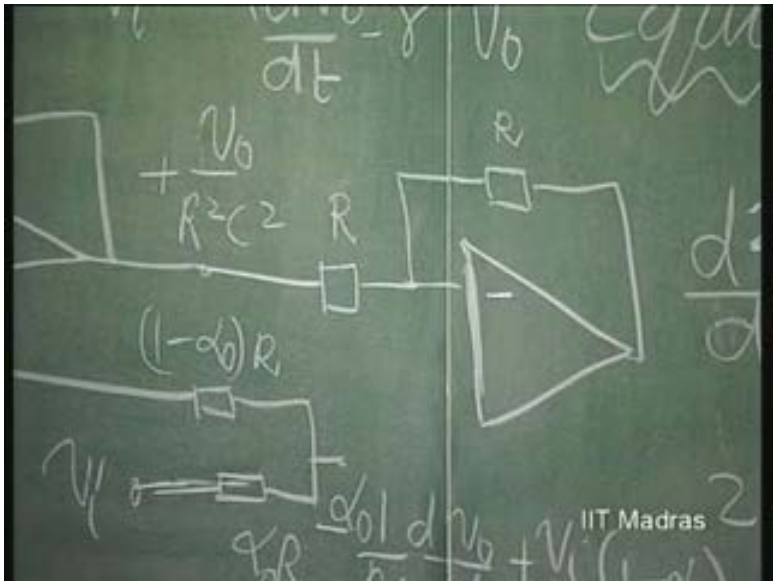

So, output will come as minus V naught by R square C square. So, this is already coming as minus V naught by R square C square. With this introduction here, this will come here and this can be connected to this. So, what happens here? Already this has been summed here. From here to here, there is a gain of 1 plus R by R; that is 2. So, these will appear at this point as 2 into 1 minus Alpha naught into V i minus Alpha naught into 2 by R C into d V naught by d t.

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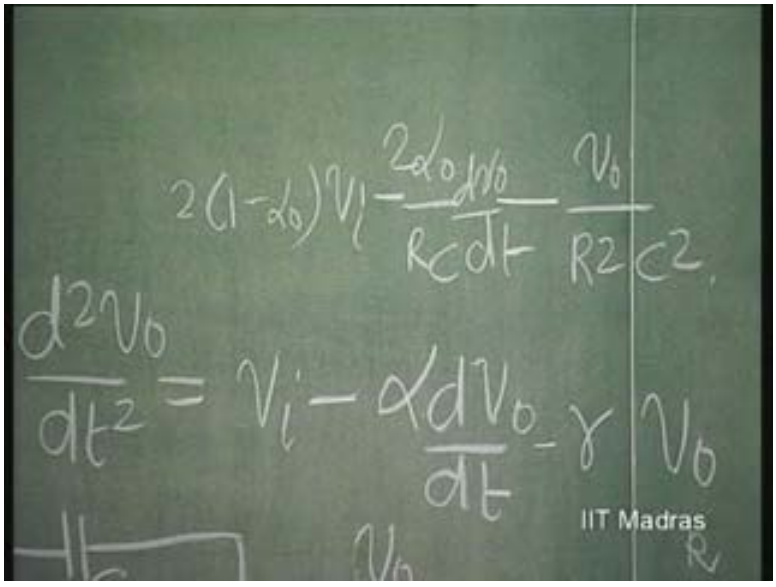

So, we can see here that essentially I have got the right hand column on this side with the proper sign except that these co-efficients have to be properly selected in order to make whatever they are. This may be made equal to 1 and this is 2 Alpha naught by R C is made equal to Alpha; and Gamma is equal to 1 over R square C square; like that you can select.

So, this is now to be made equal to d squared V naught by d t squared. That can be done because our equation says this is in fact d square V naught by d t square. So, I connect this here. So, this circuit therefore simulates this equation.

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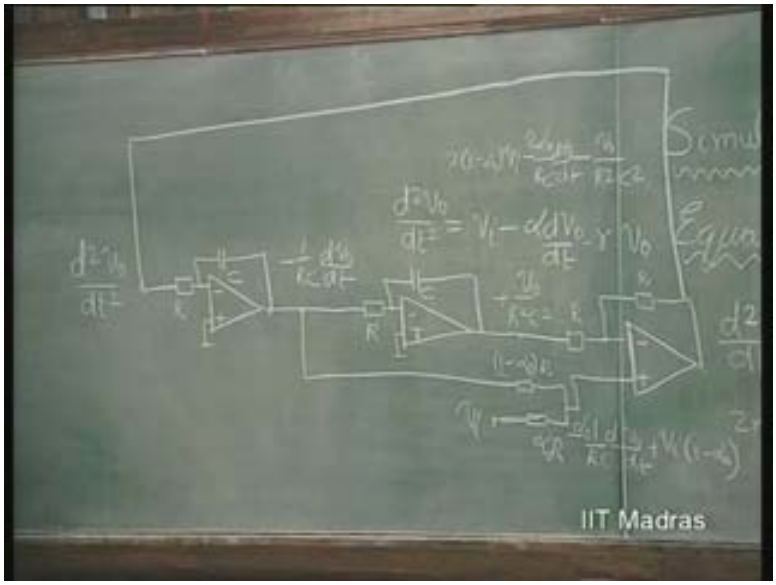

Connecting this here means, I am making the right hand side which is this, equal to the left hand side which is this, what I have assumed. So, this in fact simulates a second order differential equation and this circuit is called K H N network; that is Kerwin-Huelsman-Newcomb - K H N network or also called Universal Active Filter abbreviated as U A F. This whole thing is available as an integrated circuit.

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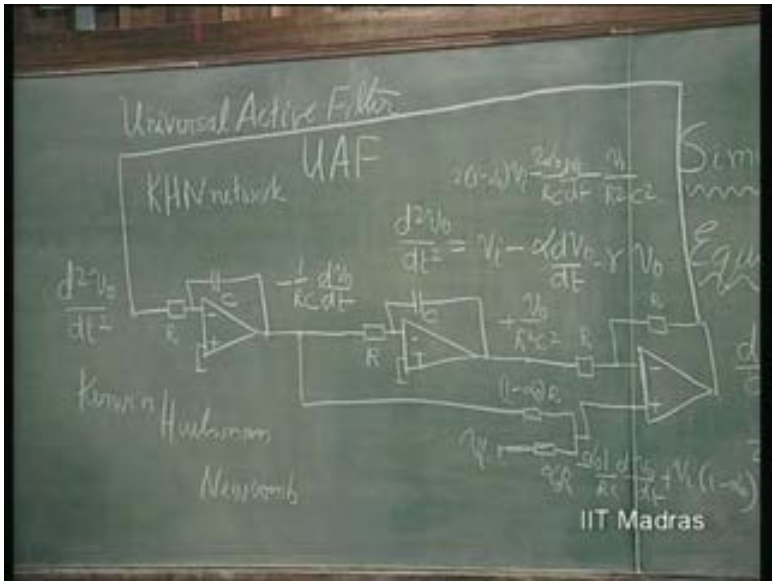

Therefore, we are now first introduced to simulation of a second order linear differential equation. We can come up with fairly arbitrary coefficient for this and simulate any second order differential equation, with Alpha and Gamma being always positive. That is, so as to have only stable solutions for the differential equation, we are restricting Alpha and Gamma to be always positive. Such a case, this differential equation will give a stable solution, transient or steady state; and the input when it is sinusoid, we can find out what the output is. The output in this differential equation, if the input is sinusoid, output is also going to be sinusoid. This sinusoidal analysis we can presently do independently and see for this circuit what are the respective transfer functions from this output to this input, this output to this input, and this output to this input.

What we just did was to start with a second order differential equation and come up with a circuit which can simulate that second order differential equation. Now we are going to analyze it using for... I mean for the analysis, the sinusoidal response.

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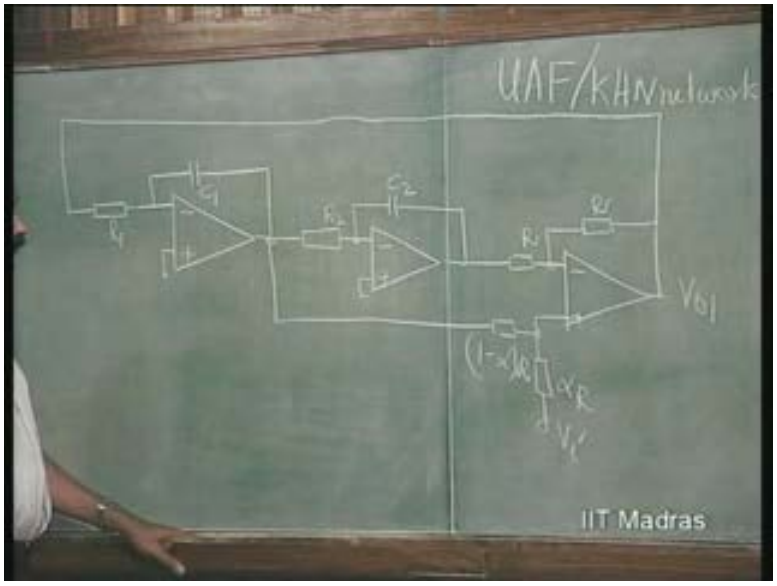

So for that, the same circuit is redrawn. We will consider this as V naught 1, this as V naught 2, this as V naught 3. Now, V naught 1 is here, this integrated. So, minus V naught 1 by S C 1 R 1 is the transfer function here; minus 1 over S C 1 R 1. Integration.

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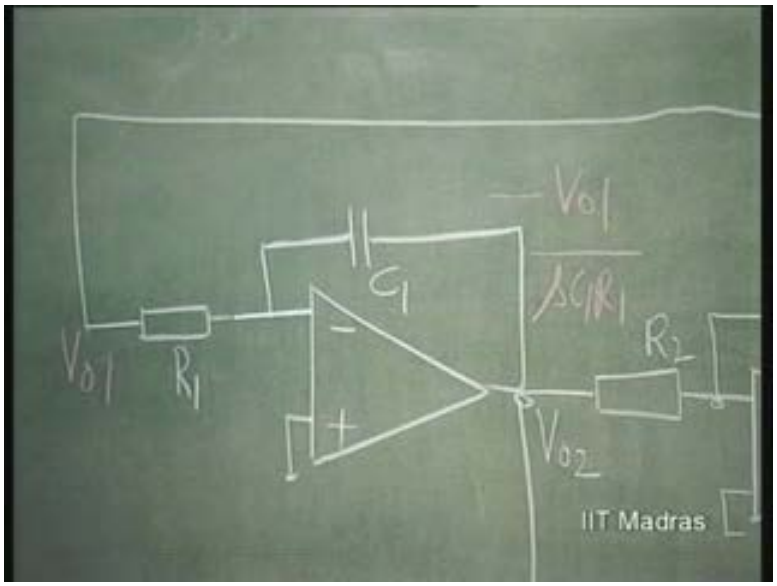

Again it is integrated once again. So, plus V naught 1 by S squared C 1 C 2 R 1 R 2. Second time integration.

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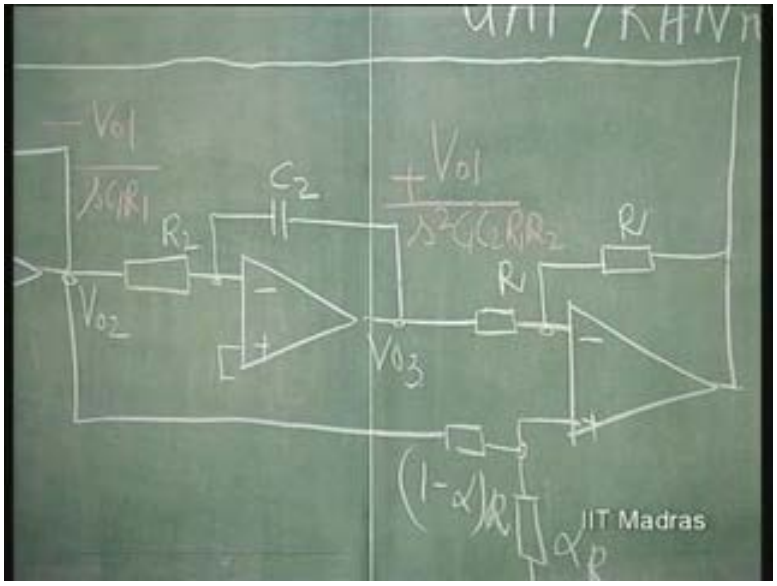

This is already minus V naught 1 S C 1 R 1. This is V i. So, what will be the V naught 1, therefore? Let us see. This minus V naught 1 will come here as Alpha times... that just as we did in the earlier equation, times minus V naught 1 by S C 1 R 1 R plus 1 minus Alpha times V i; and that gets multiplied by a factor of 2. So, you get 2 into 1 minus Alpha times V i, minus 2 Alpha by S C 1 R 1 V naught 1. And from here, it just simply gets inverted. This can be grounded.

So, minus V naught 1 by S squared C 1 C 2 R 1 R 2 and that should be equal to V naught 1. This is the same thing as d squared y by d t square being equated to something of d y by d t, something of y and something of input. So, V naught 1 into 1 plus 2 Alpha by S C 1 R 1 plus 1 by S squared C 1 C 2 R 1 R 2. This is equal to 2 into 1 minus Alpha times V i.

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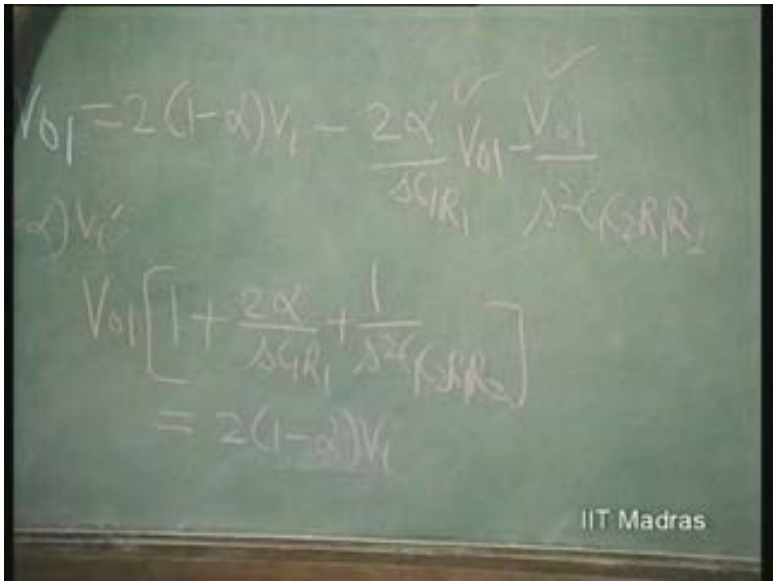

Or, V naught 1 over V i which is called the transfer function. V naught 1 over V i is equal to 2 into 1 minus Alpha divided by S squared C 1 C 2 R 1 R 2 plus 2 Alpha S C 2 R 2 plus 1 into S squared C 1 C 2 R 1 R 2. From the equation here, this is what we get.

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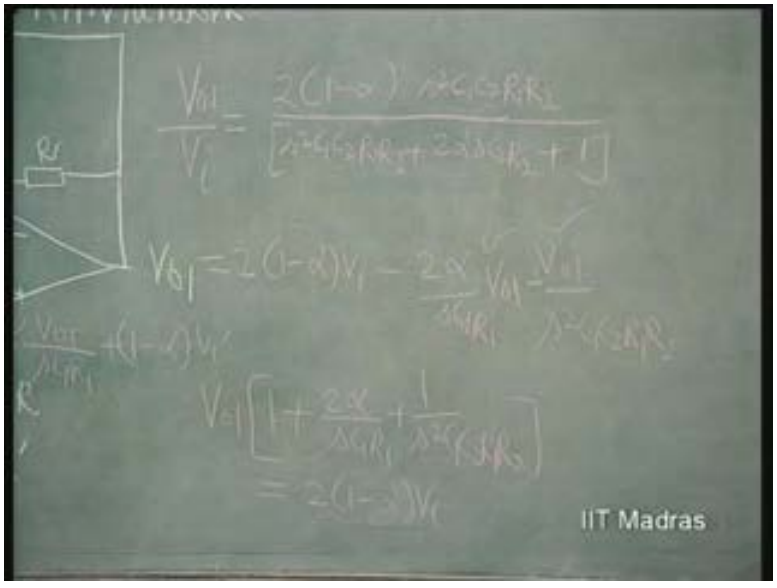

This transfer function with S squared here and S squared into something plus S into something plus 1. This is called high pass filter transfer function.

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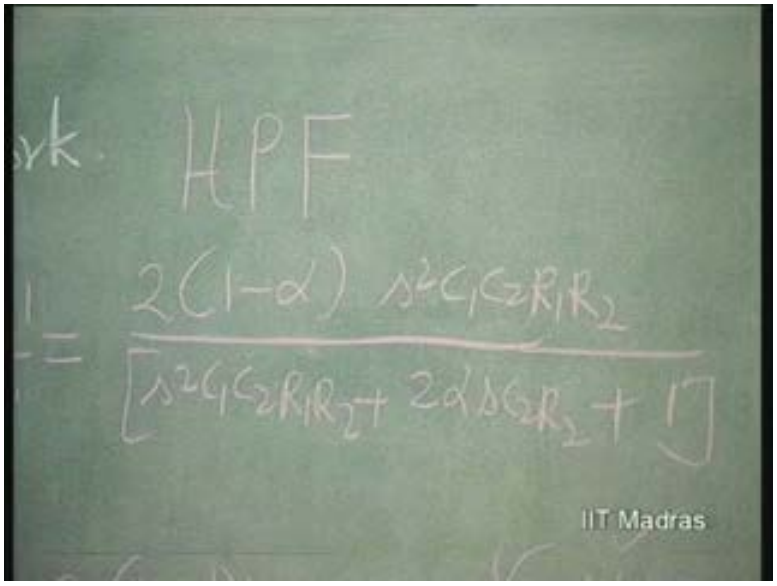

We can see that at very high frequencies, this S squared dominates. The output will be 2 into 1 minus Alpha. At very low frequencies, S equal to j Omega. Put Omega equal to zero. This is going to be zero. So, the output is going to be zero at zero frequency, goes to ultimately 2 into 1 minus Alpha at high frequency. So, it is called high pass filter.

The output is going to be like this - going to 2 into 1 minus Alpha at Omega equal to infinity.

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This is therefore high pass output. If you integrate this, the output here is going to be same; 2 into 1 minus Alpha with a negative sign because we are going to divide by S C 1 R 1 and there is a sign change.

So, you get S C 2 R 2 divided by the same denominator. So, S squared C 1 C 2 R 1 R 2 plus 2 Alpha S C 2 R 2 plus 1. This is actually zero; when S is equal to j Omega, Omega equal to zero; and zero because of S squared at S equal to infinity.

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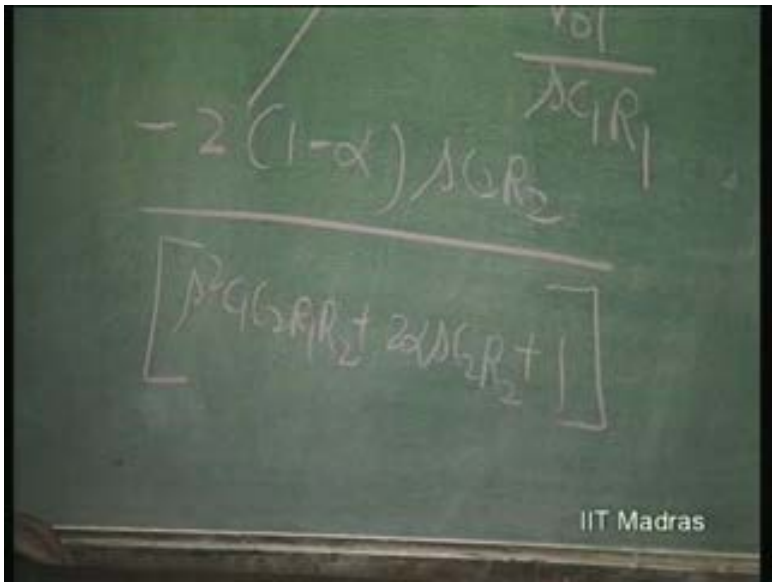

So, this is called band pass filter transfer function. Zero at S equal to j Omega, Omega equal to zero; zero at S is equal to infinity, Omega equal to infinity; and you will see that it is going to maximum when Omega naught squared is equal to 1 over C 1 C 2 R 1 R 2 because this will get cancelled with this; S S squared becomes minus Omega squared. So, 1 minus Omega squared C 1 C 2 R 1 R 2 becomes equal to zero; and this will become the highest which is minus 2 into 1 minus Alpha by 2 Alpha.

So, this depends upon 2 Alpha. If Alpha is very small, it goes to a peak. This is called resonant frequency.

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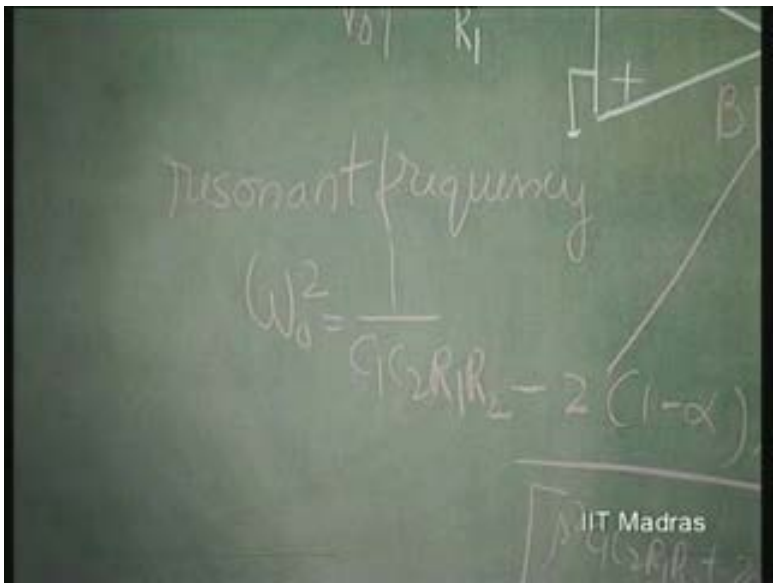

So, it becomes a peak at Omega naught squared equal to 1 over C 1 C 2 R 1 R 2. That is the band pass transfer function. Once again, you integrate. You will get this output here as...again, this sign changes to plus, divided by the same denominator and therefore that is called low pass because S equal to zero, is 2 into 1 minus Alpha; S is equal to infinity, it is zero.

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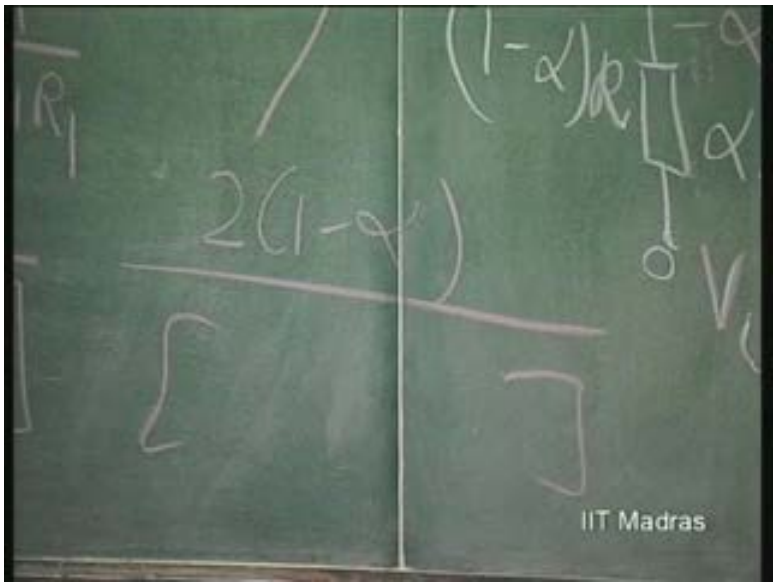

So, it is low pass. That is, it is going to be constant at 2 into 1 minus Alpha. And then, we therefore go down to zero as frequency increases. The band pass is going to look like this.

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So, these 3 outputs are simultaneously available in this case and that is why this is called universal active filter. You can get low pass here, high pass here and band pass here. A combination of these: low pass, high pass and band pass can be got by using additional summing amplifier and therefore we can gain, generate, any second order system using this simple law. And these are called poles of this system, these are called zeros. Poles of this system always lie on the negative real axis.

So, this system is always going to be stable and this is a very stable filter function and this is universally used. That is why it is called universal active filter. The whole block with additional summing amplifier is available as an integrated circuit for synthesizing any transfer function, second order transfer function, using this block.

You can use successively these blocks to generate any higher order filter functions. By cascading such filter blocks with one first order block, you are capable of getting any higher order filter block; and therefore, this is studied thoroughly so as to facilitate synthesis of any higher order filter block.