

Electronics for Analog Signal Processing - II
Prof. K. Radhakrishna Rao
Department of Electrical Engineering
Indian Institute of Technology – Madras

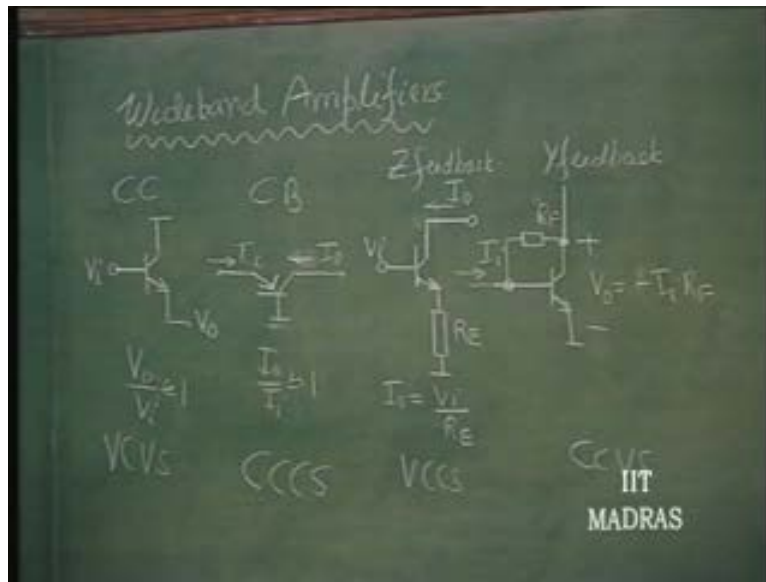
Lecture - 21
Power Amplifier

Yesterday, we discussed single stage negative feedback wide band structures. Basically, they do not need any frequency compensation; hence, the negative feedback results in wider bandwidth than otherwise. Therefore, this is a common collector stage which is essentially a voltage controlled voltage source with unity gain, normally used as a buffer stage, which is a wide band structure because of its complete negative feedback, voltage feedback.

This is common base stage which is a current control current source. The common emitter output current is totally fed back to the base. Then it results in common base structure with total current feedback and therefore I_{out} / I_{in} becomes equal to 1. So, it can be used as a current buffer just as we use this for a voltage buffer. So, this is a wide band structure.

Again, here we have Z feedback. This is Y feedback. So, this is a voltage controlled current source, current controlled voltage source. Correspondingly, the transfer parameters are written here. I_{out} / I_{in} is V_{in} / R_e , V_{out} is equal to $-I_{in} R_F$. All these are wide band structures.

(Refer Slide Time: 03:13)



And a combination of these **of these** also results in wide band structures because, if I want a voltage controlled voltage source, I will combine this with this, just as we did yesterday, and build up an IC. If I want a current controlled current source, I combine this with this; I put this first and this next...

(Refer Slide Time: 03:29)

The chalkboard contains the following handwritten text:

Combination of
these →
wide band

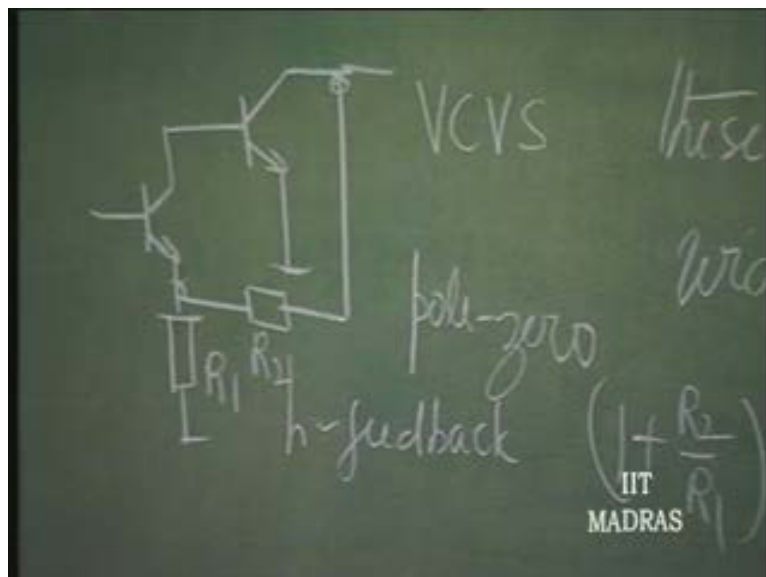
The IIT MADRAS logo is visible in the bottom right corner of the chalkboard image.

So, I can therefore build up wide band structure by combining any one of these suitably.

We have therefore negative feedback, feedback structures with 2 transistors, 2 common emitters cascaded together. What are the negative feedback wide band structures? Now, the moment you have 2 transistors, you have three time constants like input, intermediate, output; and therefore, it is likely to go into oscillations because of the three time constants; and therefore, it will need compensation. Whereas, these do not need any compensation; they retain their wide band structure even while cascading. Here, this needs compensation and therefore the compensation that we adopt here is essentially pole zero compensation, which we have discussed.

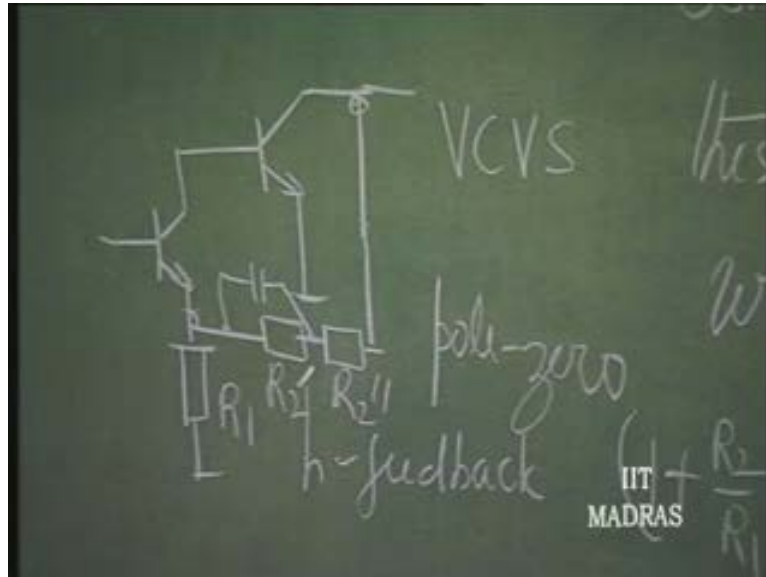
So, in the negative feedback structure also we have discussed earlier. If it is h feedback, it is this **this** structure. If it is h feedback, results in a wide band amplifier with gain equal to $1 + \frac{R_2}{R_1}$, a voltage controlled voltage source, wide band; and therefore, we can split this R_2 in a suitable manner - R_2 dash and R_2 double dash and put a capacitor across one of those so that we can adopt our pole zero compensation in order to prevent the oscillation.

(Refer Slide Time: 06:01)



So, this is what is done in the case of wide amplifier design. We will split this as, let us say, R_2 dash and R_2 double dash and provide a suitable capacitor across this so that frequency compensation can be done.

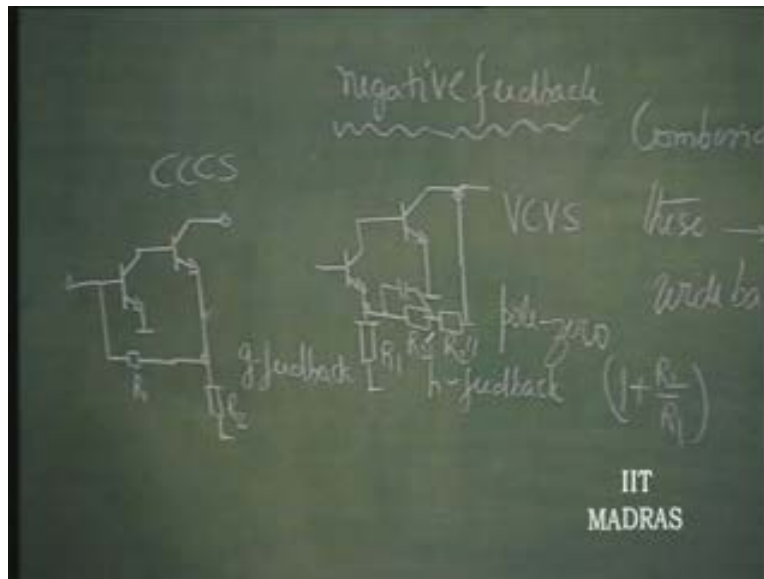
(Refer Slide Time: 06:26)



Most of the time it is very difficult to find out exactly where these poles are located; and therefore you can in any case, put...split these and put a capacitor, keep varying it until it stops oscillating, and then provide a little bit more so that there is enough margin so that at all conditions it is not going to oscillate. And therefore, this kind of compensation results in the widest bandwidth for the amplifier which is a voltage controlled voltage source.

Similarly, if it is... the same structure, you can make it a current controlled current source by g feedback. This also we have discussed earlier while discussing feedback. This will result in a current controlled current source of the same gain - $1 + \frac{R_2}{R_1}$; and therefore, this also is a wide band amplifier. Again, this might also need the same type of frequency compensation that is given in this case for making it work.

(Refer Slide Time: 07:45)



Beyond these two stages, normally...that means, connecting three amplifier stages is very difficult to make it go...work suitably as a wide band negative feedback structure because invariably, the oscillations persist. It is very difficult because the number of time constants increase to 4, minimum 4.

So, it is enough if we discuss all these amplifiers which we have already done as wide band structures. So, these wide band ICs are also available in the market as video amplifiers. So, this much about video or wide band amplifier should be sufficient for us to be conversant with how to design such amplifiers, what kind of frequency compensation we should provide, etcetera.

We have been discussing some special type of amplifiers so far which we call as wide band amplifiers or video amplifiers. In fact, whatever we have discussed in terms of bipolar structures becomes valid also for the field effect transistors; same structures. Instead of common collector, it will be common drain and common base and common gate, like that; and the feedback structures as well.

So, we will go to another special type of amplifier now. This is called power amplifier. Essentially, all amplifiers we have learned are power amplifiers; but what we discussed earlier are the ones which are normally designed at the input of a system, or pre-amplifier stages, or may be the intermediate amplifier stage. Or, they are basically small signal amplifiers where essentially the power gain is very very high; infinity basically, and the efficiency has never been considered while designing such amplifiers.

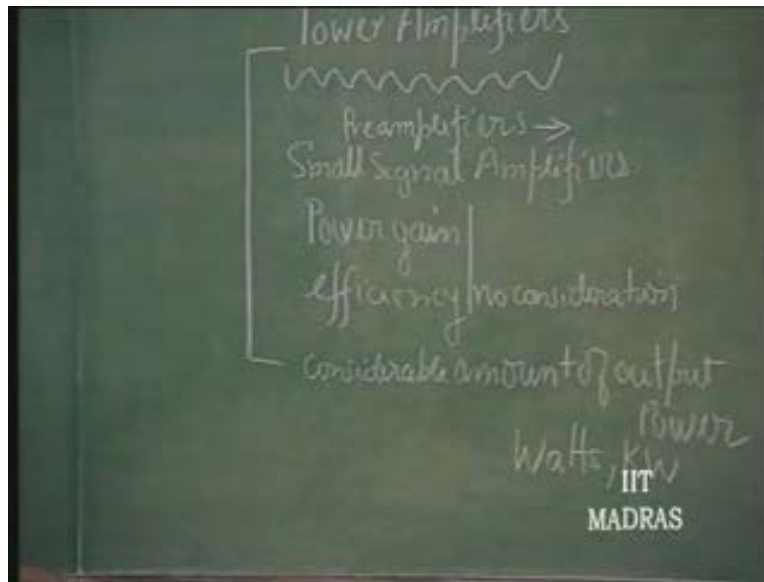
What is efficiency? After all, you feed some input power and you get power gain, huge value of power gain. How do you get this gain? The signal has low power input at the input stage of the amplifier; and output, it has been amplified considerably. This power comes from the D C bias. The D C power that is necessary to bias the active device is getting converted into the useful signal power.

Now, how much of this biasing is to be provided so that the signal power gets converted into useful power, output power? That depends upon your design, basically. We are not bothered about that initially simply because of the fact that since it is small signal, the biasing currents, etcetera, are so small that it is of no consequence. Finally, when it comes to driving a loud speaker, which...whose impedance level may be, resistance level may be of the order of few ohms, and we want watts of power, then we are now going to think of how much power we should input to the amplifier in order to get what power we require, let us say 10 watts or 20 watts. And therefore, efficiency comes into picture when we deal with final stages of amplifiers. So, these are pre-amplifiers here.

These are small signal amplifiers; efficiency no consideration. But in a power amplifier where we are dealing with considerable amount of output power of the order of may be watts; or sometimes if these are transmitters and all that Kilo watts...

So, efficiency definitely will come into picture; how much power we have to input in order to get this much of signal power. So, watts and Kilo watts of power. So, how... what are these amplifiers that we have already discussed?

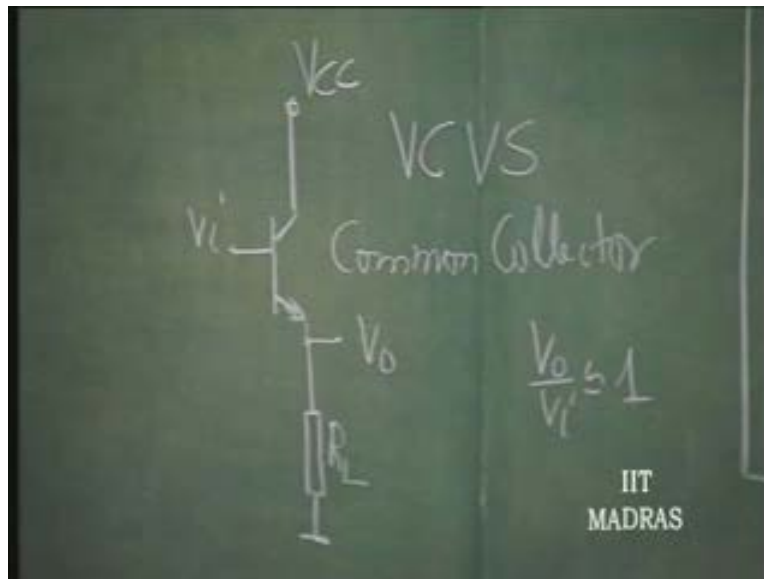
(Refer Slide Time: 13:48)



Let us consider a power amplifier, its characteristics. Let us consider a common collector stage because this is basically a good voltage controlled voltage source; can also act as a buffer stage. Since our load is going to be, I said, may be a speaker or something like that, and therefore the load is going to be of the order of few ohms, we do not want our previous stage to be straightaway loaded by these few ohms. So, they...we put a buffer stage here.

So, the load is going to be R_L here. This is V_{cc} , let us say; this is grounded and the output here... if this is V_i , the output here V_{out} is going to be very nearly equal to V_i . This is sinusoidal varying. This also will vary sinusoidally. The gain of this is very nearly equal to 1. This is a commonly used power amplifier stage. The input power is small because the input current is of the order of $\beta + 1$ - less than the output current. This is the output current.

(Refer Slide Time: 15:39)



So, input power is going to be much less than the output power. That is definitely true. And what is going to be the output power, what is efficiency, etcetera, we will try to understand in terms of this. Apart from this efficiency part, power gain is an important thing. Efficiency. The other thing of importance in power amplifier is... in fact, this is important in all amplifiers but in power amplifiers this is all the more important because the load is going to be pretty small. If it is voltage amplifier, the load is going to be pretty small.

So, distortion is significant particularly because the signal levels are high, whether it is voltage or current; and we cannot consider the amplifier as a small signal amplifier at all. We cannot do the analysis of this kind of thing that we have done in the previous stages; replace the thing by a small signal equivalent. It is not, because the signal is varying considerably; and therefore in power amplifier analysis, it is futile to discuss about distortion without considering the non-linear aspects of the device. So, the non-linear aspects of the device comes into picture.

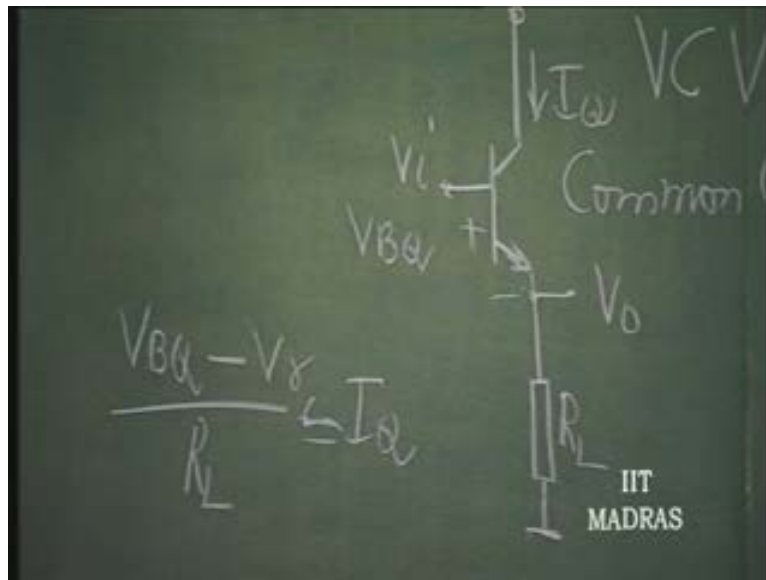
If it is a feedback structure, the non-linearity is automatically reduced. Here, $V_o \approx V_i$ is valid for large signal also. So, that is why we have chosen for an

illustration, a structure which is basically having low distortion. We have to find out the efficiency and power gain of this structure.

Now, we say that in order to make this operate for signal which is going both positive and negative, A C signal, we have to operate it at a quiescent point. So, we know that this is having some I_{Q} quiescent. Obviously, we have V_{BQ} quiescent here in order to make this operate at I_{Q} quiescent.

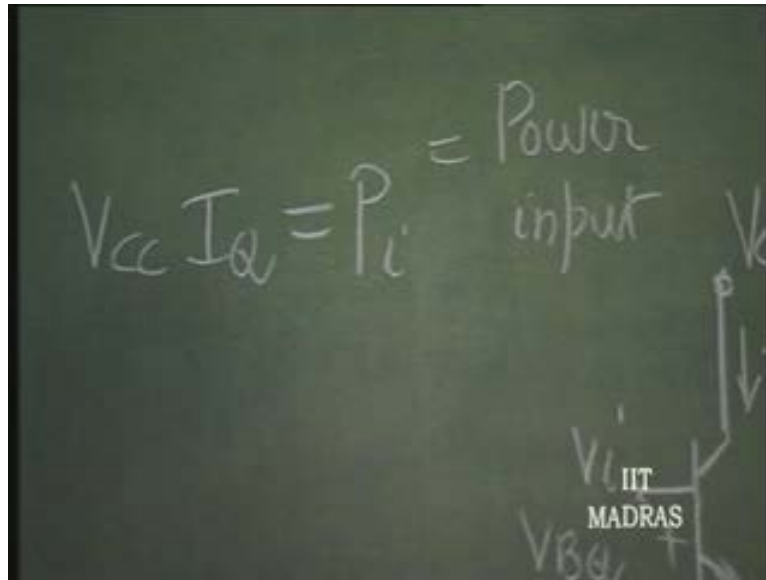
So, V_{BQ} quiescent minus V_{γ} - this one, divided by R_L in this case is I_{Q} quiescent. Please understand this. This is the D C voltage. In order to make this work at I_{Q} quiescent, I have to apply this much D C voltage - V_{BQ} quiescent, minus V_{γ} divided by R_L will be very nearly equal to... There is no point in considering Alpha, etcetera, in this case because Alpha, we will consider as unity.

(Refer Slide Time: 18:37)



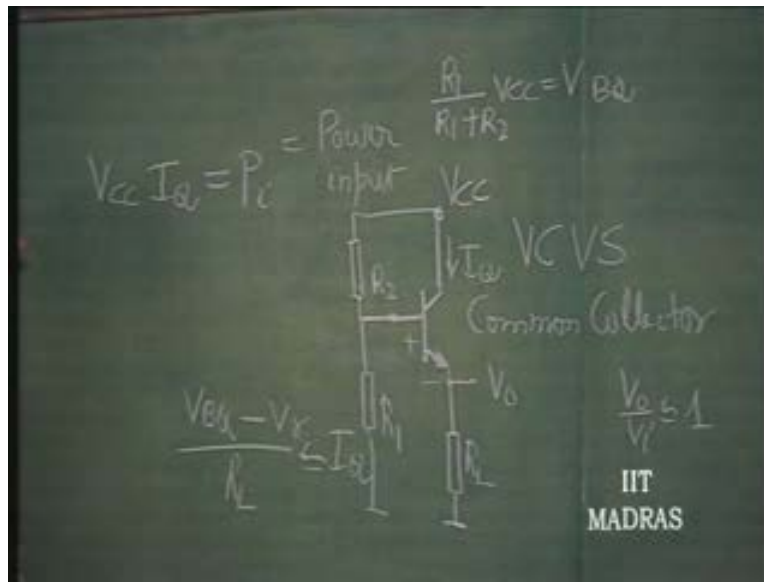
So, this is the quiescent current in this. Therefore, even when there is no signal applied, this is dissipating power. What is the power dissipated in the whole of this structure? It is nothing but V_C into I_Q . This is the power input. So, we will call it P_i ; so, the power input.

(Refer Slide Time: 19:23)



This current being Beta times less, the biasing circuits, etcetera, if they are needed here for example... How do you get V_{BQ} ? You can put, may be, a resistance arrangement here. This we have already discussed earlier. Thevenin's voltage you can generate by putting R_1 here and R_2 here and making R_1 by R_1 plus R_2 times V_{cc} equal to V_{BQ} . This, we have discussed earlier. So, this is the biasing arrangement for this power stage.

(Refer Slide Time: 20:10)



What I am trying to say is the total current is I_Q plus the current drawn from here, which is V_{CC} divided by R_1 plus R_2 . So, actual power input is not only this plus V_{CC} into V_{CC} by R_1 plus R_2 ; this is in fact the total power dissipated in this whole so called power amplifier stage. This is required for biasing the transistor.

(Refer Slide Time: 20:45)

The handwritten equation is:

$$\frac{V_{CC} V_{CC}}{R_1 + R_2} + V_{CC} I_{BQ} = P_i =$$
 Below the equation, the word "biasing" is written.

This is going to be pretty low. By selecting R_1 plus R_2 large, not too large, because this current V_{cc} by R_1 plus R_2 , this should be definitely much greater than the base current. We have ignored that base current. That means this current V_{cc} by R_1 plus R_2 should be definitely greater than I_Q divided by β . This is, let us say, β_{min} , worst case.

(Refer Slide Time: 21:27)

The image shows a chalkboard with the following handwritten equation:

$$\frac{V_{cc}}{R_1 + R_2} > \frac{I_Q}{\beta_{min}} - \frac{V_{BQ}}{R_L}$$

The text "IIT MADRAS" is visible at the bottom right of the chalkboard.

So, you have to select R_1 plus R_2 larger than this condition; and it should be obviously less than... V_{cc} by R_1 plus R_2 should be much greater than or much less than I_Q . This is the way you have to select because I_Q is anyway necessary to bias this transistor; and I_Q must be greater, much greater than V_{cc} by R_1 plus R_2 .

(Refer Slide Time: 21:51)

$$\frac{V_{CC}}{R_1 + R_2} = \frac{I_{CQ}}{\beta_{min}}$$
$$V_{BE} = I_{CQ} R_L$$

IIT
MADRAS

If we select all that, then we can say that input power is essentially V_{CC} into I_{CQ} , approximately.

(Refer Slide Time: 22:24)

$$V_{BE} V_{CC} + V_{CC} I_{CQ} = P_i = P_o$$

$R_1 + R_2$ biasing

$$P_i = V_{CC} I_{CQ}$$

IIT
MADRAS

This is an illustration of how any power stage has to be designed. If the power transistor is operating at I_{CQ} , rest of the current that is drawn for biasing purposes should be much

less than that current; and the corresponding resistance, etcetera, are chosen in the...in that manner.

So, this gives an idea as to how this power stage is now designed. This aspect of deciding about all these currents were of trivial nature when we were designing this so called small signal amplifier. We never bothered about that and we never bothered about the power input at all. That was because the I_Q was very small compared to what was necessary in the case of a power stage which is the final stage. Now, if it is having I_Q flowing through this, what is the signal swing here?

I_Q . I am applying a V_i here and V_{naught} is very nearly equal to V_i . Let us say V_i is a sine wave. What is the maximum value of V_{naught} you can have? V_i will vary here as I_Q plus or minus I . Because of the signal, this signal current will be super imposed over the quiescent. So Δi can be made equal to minus I_Q . That we had discussed earlier also so that the total current becomes equal to zero on one side. So on one side, the current can go down to zero. The instantaneous value of current can go down to zero because as signal is applied, this current is going to be, instantaneous current is going to be, increasing or decreasing here. So, this is going to be either equal to zero or on the other side, it can keep on increasing. There is no limit actually. As long as V_i keeps on increasing this current can keep on increasing, without any limit.

Now, what is the maximum current ultimately it will lead to where V_i becomes, may be, almost up to V_{cc} , because this might be coming from the previous stage and previous stage is also connected to a supply like V_{cc} . And therefore, the maximum voltage you can have there is at most equal to...peak voltage is V_{cc} . So, this can go...this base voltage can go up to V_{cc} .

If the base voltage goes up to V_{cc} , this voltage can go up to V_{cc} minus V_{γ} ; and therefore V_{naught} , the highest value of V_{naught} , can be V_{cc} minus V_{γ} .

(Refer Slide Time: 25:15)



If V_{CC} is large compared to V_{γ} , if V_{CC} is very large compared to V_{γ} , this is V_{CC} itself. So, we can have the V_{CE} peak equal to $V_{CC} - V_{\gamma}$, which is very nearly equal to V_{CC} and I_{peak} corresponds to... actually I_{peak} we will put it; I_{peak} corresponds to I_Q itself.

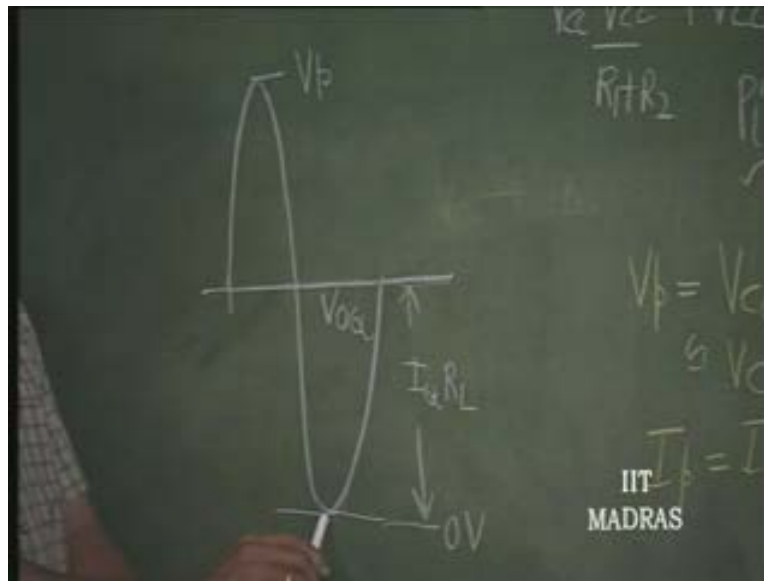
(Refer Slide Time: 26:31)

$$V_p = V_{CC} - V_{\gamma}$$
$$\leq V_{CC}$$
$$I_p = I_Q$$

Therefore, current swing... on one side, current swing is the one that limits; on the other side, voltage swing is the one that limits.

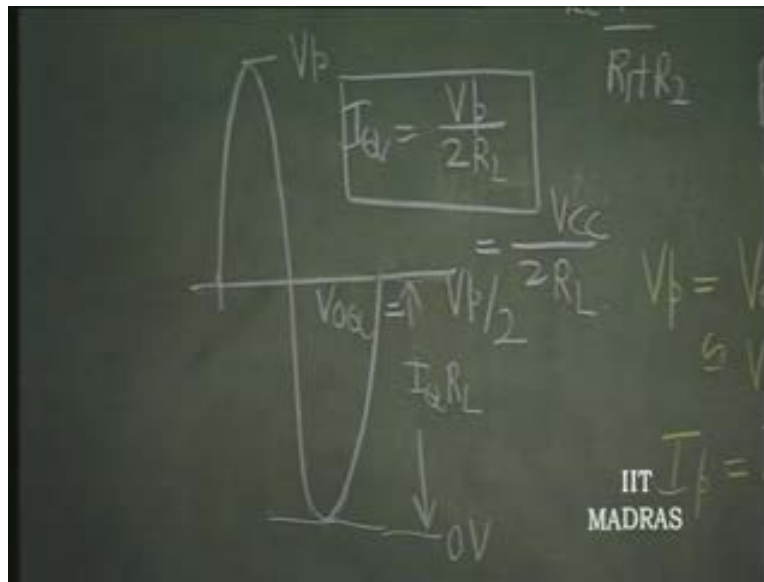
So, if we want now equal swing on either side of the quiescent, let us see... If it is a single side, the quiescent is here, $V_{naught Q}$; and on this side, it can go almost up to V_p . Actually, it is V_p minus V_{gamma} . On the other side it can go up to zero. When the instantaneous value of current through the load becomes equal to zero, instantaneous value of voltage also is zero.

(Refer Slide Time: 27:11)



So, it goes from zero all the way up to V_p . So, if it is to be symmetric, obviously, $V_{naught Q}$ has to be equal to V_p divided by 2. It is to be symmetric. This is V_p by 2 and that is V_p by 2. So, if this is... $V_{naught Q}$ is V_p by 2 and $I_Q R_L$ is equal to that. So, $I_{quiescent}$ is already fixed for the best operation as V_p divided by 2 R_L . V_p by 2 divided by R_L so that... This is because I_Q into R_L is now V_p by 2. So, quiescent current is V_p by 2 R_L ; or V_p is equal to V_c divided by 2 R_L .

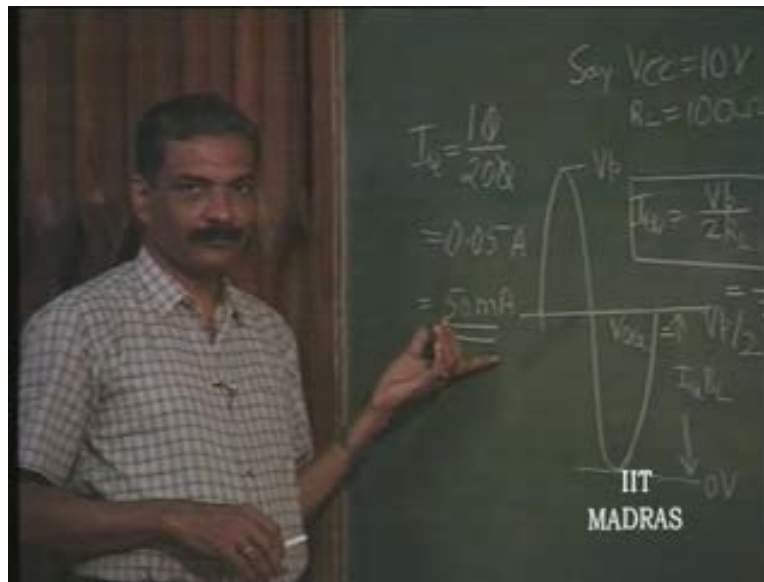
(Refer Slide Time: 28:10)



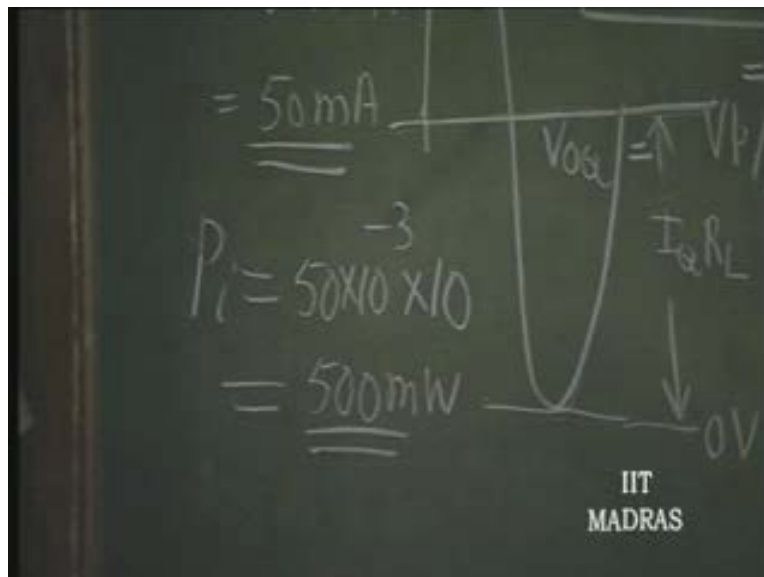
So, we said V_p is very nearly equal to V_{CC} , under the best situation. So, V_{CC} by $2R_L$. So if, let us say, supply voltage is 10 volts and R_L is, let us say, 100 ohms, 10 volts, 100 ohms, then this will...current will be 10 volts divided by 200 ohms. So, let us say, if V_{CC} is 10 volts, R_L is 100 ohms, then I_Q is going to be 10 by 200 ohms which is point zero 5 amperes or 50 milliamperes.

Now you can see the kind of operating current I should have just for this load of 100 ohms with supply voltage of 10 volts, in order to have symmetric swing going up to...all the way up to half the value - that is 5 volts, I have to have operating current of 50 milliamperes.

(Refer Slide Time: 29:42)



So, if 50 milliamperes is the current then what is the power input? Power input is going to be 50 milliamperes into 10 volts. So, that is going to be 500 milliwatts or point 5 watts.



This point 5 watts of power is continuously wasted. Suppose you are using a battery there even when the signal is not coming, this power is being wasted. So, this is why it is inefficient.

In order to keep it in readiness for a swing which is going to be coming may be sometime or other, we are not sure whether this much swing is going to occur at any time, we are now wasting 500 milliwatts of power, just waiting for the signal to come.

So please... This is what is called as class A operation.

This kind of operation where, in order to receive, let us say a King. You are receiving the King. You do not know when the King is going to arrive. So, in order to prepare him, in order to prepare yourself to receive him, you are continuously wasting certain amount of money. All the welcoming party, the band, the decoration, all of them have to wait, keep waiting; and they are going to spend only few minutes may be, just playing their band, when the King arrives.

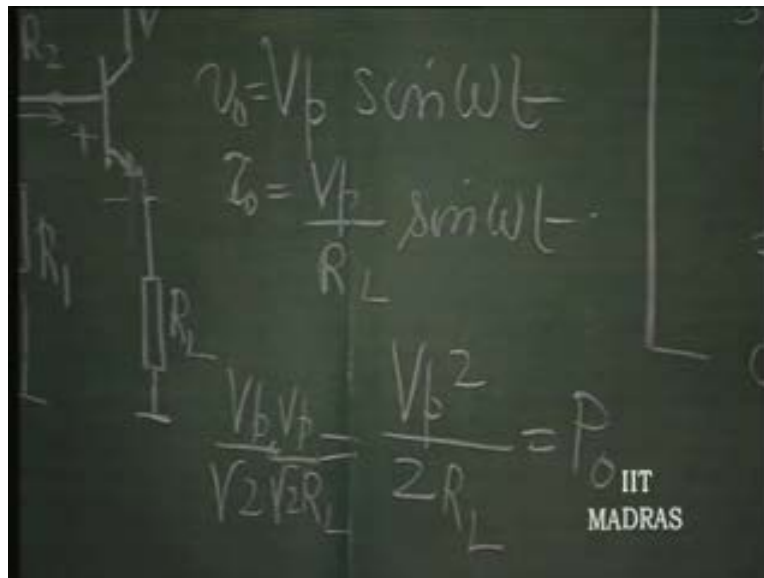
But, since the time is not known to you, may be you have to wait for 24 hours or 48 hours, who knows? So, this is what is called as class A operation. This is an inefficient way of operation. What is the best way? We can say the King is coming but the time is not known. But the moment the King comes, we will be woken up. So, the bandwallas and the reception committee, all of them are given a chance to sleep. The moment the King comes, they will wake up and then start playing the band. That is really what is called as class B operation. That you will be sleeping and only when the signal comes you are getting ready.

So, class A operation is an inefficient way of power amplification. Now, let us see what is the efficiency? Under the best condition, what the efficiency is? The signal has to be... for the efficiency to be maximum, signal has to go up to V_{cc} because maximum power has to be dissipated in the load. What is the power dissipated in the load? Let us discuss this.

If it is a symmetric swing and the voltage is $V_p \sin \omega t$, the current is going to be... this is the voltage across the load and the current is going to be V_p divided by $R_L \sin$

ωt . This is the current; that is the voltage. Then the power dissipated in this is going to be V_p divided by $\sqrt{2}$, r m s value, and V_p by R_L divided by $\sqrt{2}$. So, V_p square divided by $2 R_L$. V_p divided by $\sqrt{2}$, V_p divided by $\sqrt{2}$ into V_p by R_L by $\sqrt{2}$, which is V_p square by $2 R_L$ is the power output; at any time.

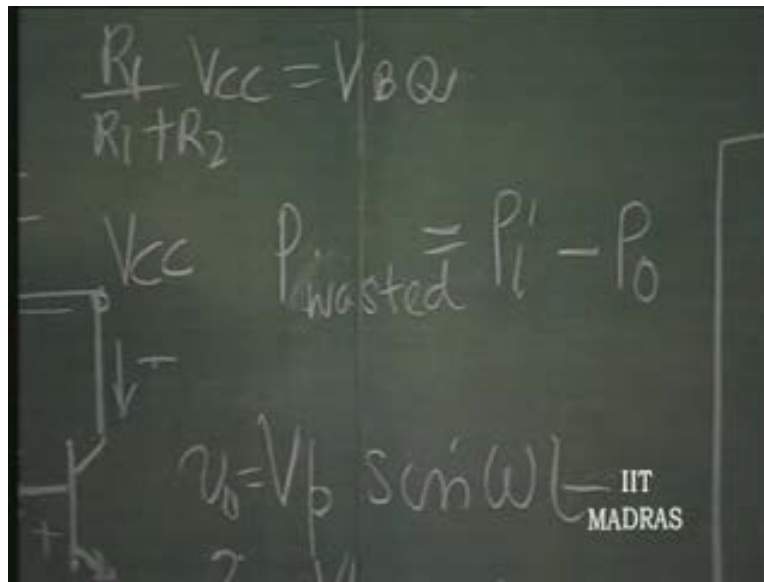
(Refer Slide Time: 34:19)



If there is sine wave input at... output is going to be a sine wave and therefore at any time the power outputted is V_p square by $2 R_L$. What is maximum power outputted? When V_p becomes equal to V_{cc} , the peak value.

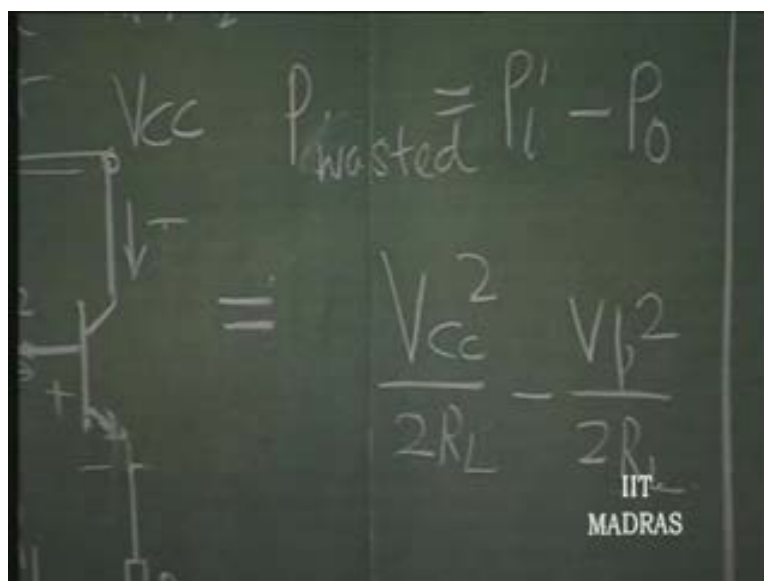
Why should we take the maximum power? We know that the power dissipated in the transistor. That is power dissipated in the transistor as well as the resistor. Rest of the circuit, power wasted, let us say, is nothing but power inputted minus output power...

(Refer Slide Time: 35:16)



What is the power inputted? Let us see. Power inputted is going to be V_{CC} ; that is the DC, into IQ because AC is not going to cause any power. The IQ, IQ is already decided as V_{CC} divided by $2R_L$. This, we have already decided. V_{CC} divided by $2R_L$. So, this is going to be V_{CC}^2 divided by $2R_L$; and output power is V_p^2 divided by $2R_L$.

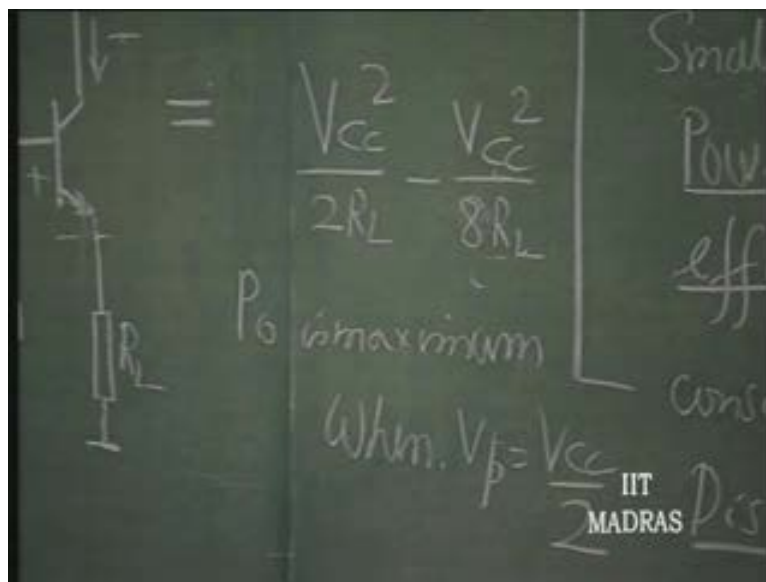
(Refer Slide Time: 36:18)



And what is the value of V_p ? V_p at which you get maximum output power is going to be V_{cc} divided by 2. On one side, it can go up to V_{cc} by 2; on the other side, it can go up to V_{cc} by 2.

So, power wasted is minimum only when this is maximum. Otherwise, let us say, power wasted is fully the power inputted when the signal is not there. The entire thing is wasted in this circuit as DC power. Now this DC power gets converted into some amount of useful power and the amount of useful power is maximum when V_p is equal to V_{cc} by 2. So, this becomes V_{cc}^2 by 4, $8 R_L$. So, power output is maximum when V_c , V_p is equal to V_{cc} by 2.

(Refer Slide Time: 37:45)



On one side it can go... if this is V_{cc} by 2, on one side it can go up to V_{cc} . On the other side, it can go up to zero. So, it is V_{cc} by 2; and therefore that much power is wasted in the circuit.

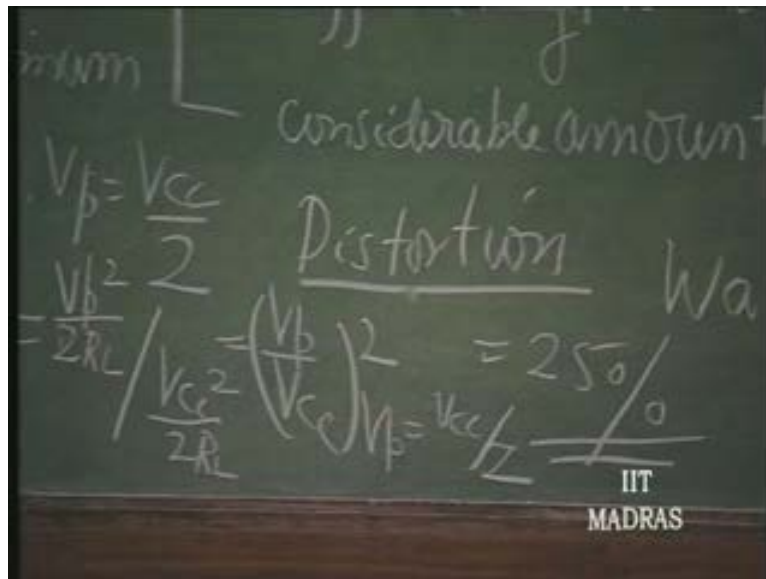
Efficiency is defined as... this is efficiency. Power outputted divided by power input. This is going to be the maximum efficiency. If you say η_{max} , you have to consider the maximum output. Input is constant. V_{cc}^2 by $2 R_L$. So actually speaking,

generally this is V_p^2 divided by $2 R_L$. V_p^2 divided by $2 R_L$ divided by V_{cc}^2 divided by $2 R_L$; or this is V_p by V_{cc} whole square generally; and since the maximum value of this, **maximum value of this** occurs when V_p is V_{cc} by 2, the efficiency is only, maximum efficiency is only how much? 25 percent.

So, let us understand this very clearly. Maximum efficiency of this class A stage as given here is 25 percent. Such is the case of any class A stage. I have used for demonstration, only common collector stage. Even if you use common emitter stage with load here, such is the case.

So, it is of no difference what kind of stage I use, whether it is FET or bipolar. As long as it is class A, the maximum efficiency of such a stage is always going to be less than 25 percent because this is only the best efficiency possible; and it is not possible for us to have the signal always at V_p . It is going to change. Signal is going to keep changing depending upon your output. So, this is, may be an audio signal.

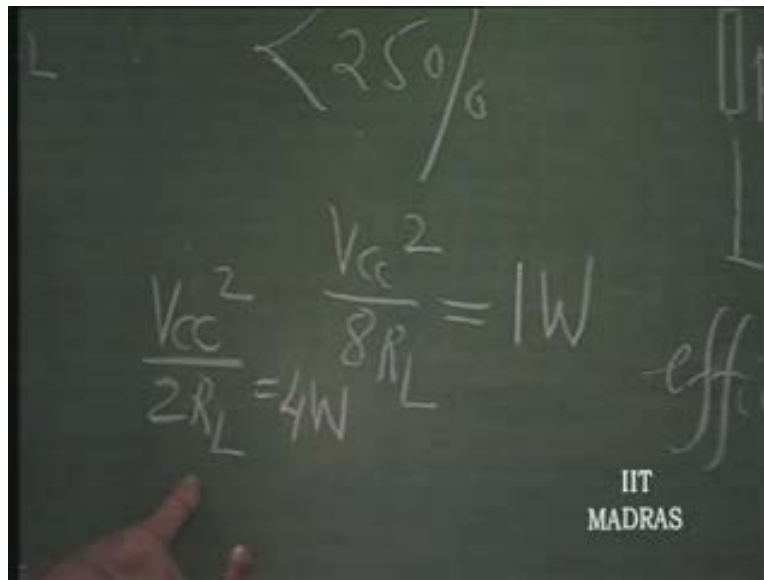
(Refer Slide Time: 40:33)



So, at best, it may...can reach V_p at a certain given moment. That is all. So, this is always less than 25 percent. What does it mean? If I want this 25 percent, that is this

power, V_{cc} squared by $8 R_L$ to be... V_{cc} squared by $8 R_L$ to be... this is the useful power, let us say, 1 watt. Then, V_{cc} square by R_L , V_{cc} square by $2 R_L$ is going to be 4 watts. That means, the quiescent power I must be prepared to waste is 4 watts, in order to get a power of 1 watt output. this 4 watt is going to be dissipated continuously, when signal comes. And that also when it reaches its peak value. Then only you are able to get a 1 watt output; and then 3 watts is the output dissipated in the stage.

(Refer Slide Time: 41:53)



So, you can therefore imagine the amount of heat sinking and all that thing that is required for the device or the circuit itself. This 4 watts is to be dissipated in the circuit. How much is going to be dissipated in the resistance, how much is going to be dissipated in this? That is, half is going to be dissipated in the resistance, half is going to be dissipated in the transistor.

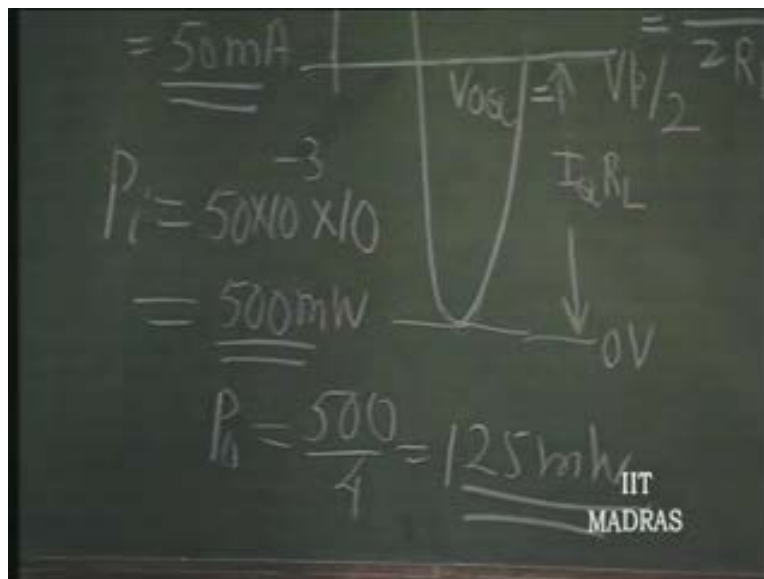
If 4 watts is the quiescent power and this is V_{cc} by 2; so, V_{cc} by 2 square divided by R_L is dissipated here and the rest of it is dissipated here. So, 2 watts will be dissipated here and 2 watts will be dissipated here. Other... the signal situation, it will dissipate less because some of the power is converted into this thing.

So, the transistor that you have to use for delivering 1 watt should be 2 watts; but the circuit actually is going to dissipate 4 watts under quiescent situation because that is a D C power that is going to be dissipated here.

So, this D C current is flowing in addition to the A C current. There will be some amount of D C power continued to be dissipated even when the A C is there. So, this particular transistor and this resistor, both of these things are dissipating maximum amount of power, when the signal is not there. When the signal is there, some amount of that power is getting converted into signal power, useful power, A C power.

Now, for this example of V C C is equal to 10 volts and R L is equal to 100 ohms, you have seen that 50 milliamperes is the current; and we can also find out what the... this power inputted is - 500 milliwatts. That means from this, you can only get one fourth of this power as signal power. That means, output power could be under the best situation, one fourth of 500. Is this clear?

(Refer Slide Time: 44:56)



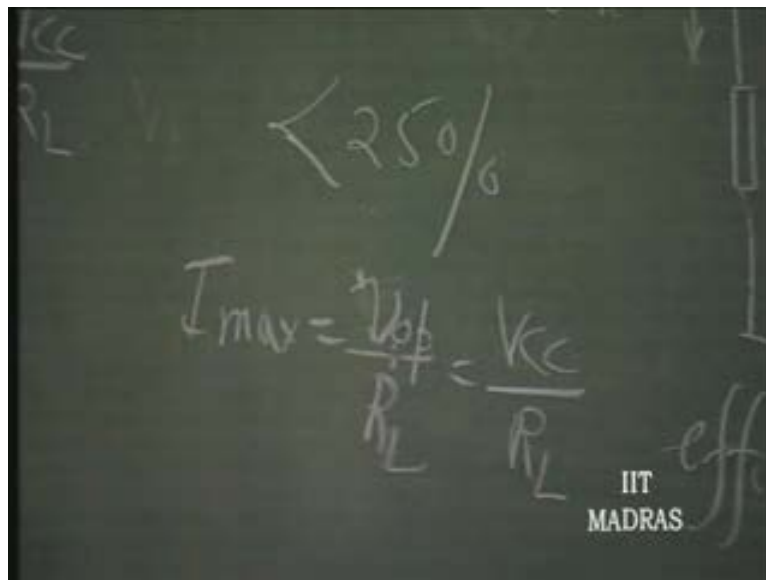
Similarly, if you have to design for a specific output power, you can find out what should be the quiescent input power and based on that, you select the transistor and the load.

Load is normally given to you. It may be a speaker. So, you select the corresponding transistor based on this.

What are the other factors which are important? In power stage, apart from this, power that is to be dissipated in the active device. The current is also important and the voltage. The maximum current is the peak current when this voltage goes to V_{cc} . That is V_{cc} itself.

So, the maximum current in this circuit I_{max} is going to be V_p divided by R_L which is V_{cc} . In fact, instantaneous value of V_p . So, V_{peak} . So, that is V_{cc} itself. So, V_{cc} divided by R_L .

(Refer Slide Time: 46:14)


$$I_{max} = \frac{V_{cc}}{R_L} = \frac{V_p}{R_L}$$

250%

IIT
MADRAS

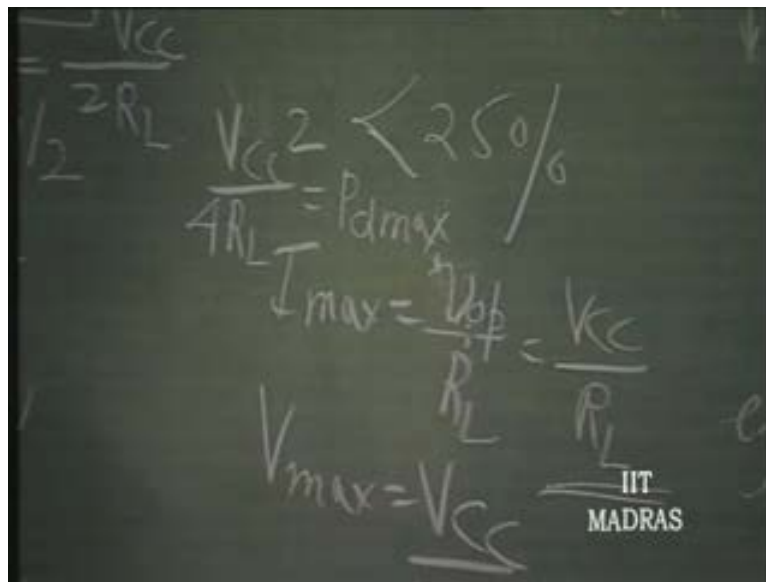
This is the point at which maximum current, load current, is going to flow. The instantaneous value of voltage is V_{cc} . That divided by R_L is the maximum current. That current has to flow through the transistor as well. So, your transistor rating should be better than V_{cc} by R_L . This is the maximum current; and the maximum voltage across the transistor is V_{cc} itself, when this voltage goes down to zero.

So, maximum voltage and maximum power is going to be determined by...this is V_{CC} square divided by $2 R_L$. That is the input power. Half of it is going to be V_{CC} square divided by $4 R_L$. That is the maximum power to be dissipated in the transistor.

When the voltage here increases, the current decreases; when the voltage decreases, current increases. So, the maximum power under the quiescent situation is V_{CC} square divided by $4 R_L$. Therefore, for the transistor, this is...

So, the active device - it is V_{CC} square divided by $4 R_L$. So, based on all these factors, you will select the transistor that is necessary for this.

(Refer Slide Time: 48:05)



Let us now summarize what we have learned so far. In class A power amplifier, given a supply voltage of V_{CC} and load of R_L , we have connected a transistor in series with this so that we can control the power in R_L ; or, we can get the output power in R_L . So, P_i is equal to always V_{CC} into quiescent current in this. P_d at that point of time, when signal is not applied, gets dissipated in the transistor and the load. So, P_d in general is nothing but V_{CE} , voltage across the transistor into current through the transistor; V_{CE} into I_Q . P_d through the load is V_{CC} minus V_{CE} into I_Q . For maximum output swing on the

other hand, V_{CE} we wanted to make it equal to V_{CC} divided by 2. Then, I_Q becomes equal to V_{CC} by $2R_L$.

(Refer Slide Time: 49:13)

Handwritten equations on a chalkboard:

$$P_d(\text{Trans}) = V_{CE} I_Q$$
$$P_d(\text{load}) = (V_{CC} - V_{CE}) I_Q$$

for maximum output swing

$$V_{CE} = \frac{V_{CC}}{2} \quad I_Q = \frac{V_{CC}}{2R_L}$$

IIT
MADRAS

And, another situation, P_d is going to be V_{CC} square by $4R_L$ in both load and transistor. This is a DC power dissipated both in the load and transistor. Ultimately therefore, P_i is sum of these two powers which is supply voltage into quiescent current and that is V_{CC} squared by $2R_L$. Half of it gets dissipated here in the transistor; half gets dissipated in the load.

(Refer Slide Time: 49:37)

Transistor

$$P_i = V_{CC} \frac{V_{CC}}{2R_L}$$
$$= \frac{V_{CC}^2}{2R_L}$$

IIT
MADRAS

Then, under signal input situation, V_{naught} is $V_p \sin \omega t$; I_{naught} is $V_p / R_L \sin \omega t$; and P_{naught} is $V_p^2 / 2R_L$. Under this, $I_{naught} Q$ continues to flow, D C current continues to flow and D C dissipation in the load continues to be the same. So, this dissipation remains the same.

(Refer Slide Time: 50:09)

$P_d = \frac{V_{CC}^2}{4R_L}$

in both load & Transistor

$$P_i = V_{CC} \frac{V_{CC}}{2R_L}$$

IIT
MADRAS

Some of the transistor active device dissipation on the other hand gets converted into useful signal power. So, transistor dissipates less power during active cycle and that power is given out in the load as the useful power. That is how the active device is responsible to convert its D C power into signal power.

So if, let us say, we have the input power equal to 100 watts. Initially, 50 watts will be dissipated by this and 50 watts will be dissipated by this; and the maximum signal output power you can get when you have 100 watts is 25 watts. At that time, 75 watts is going to be still dissipated in the circuit goes waste, out of which, actually... earlier 50 watts was getting dissipated here and that 50 watts continues to be dissipated. Then this is going to dissipate further D C power of 25 watts.

This 25 watts which was earlier getting dissipated as D C power is getting converted into A C power. So, that is why this active device is responsible for converting the D C power into A C power.