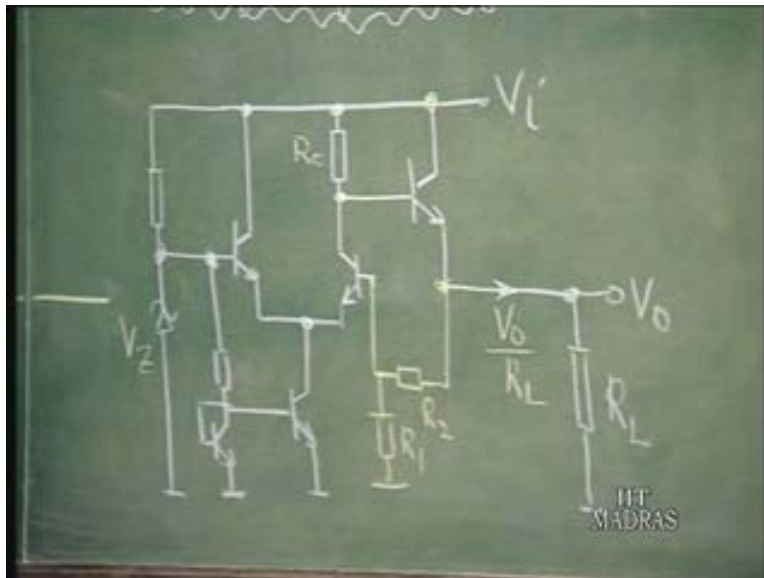


Electronics for Analog Signal Processing - II
Prof. K. Radhakrishna Rao
Department of Electrical Engineering
Indian Institute of Technology – Madras

Lecture - 28
Voltage Regulators (Continued)

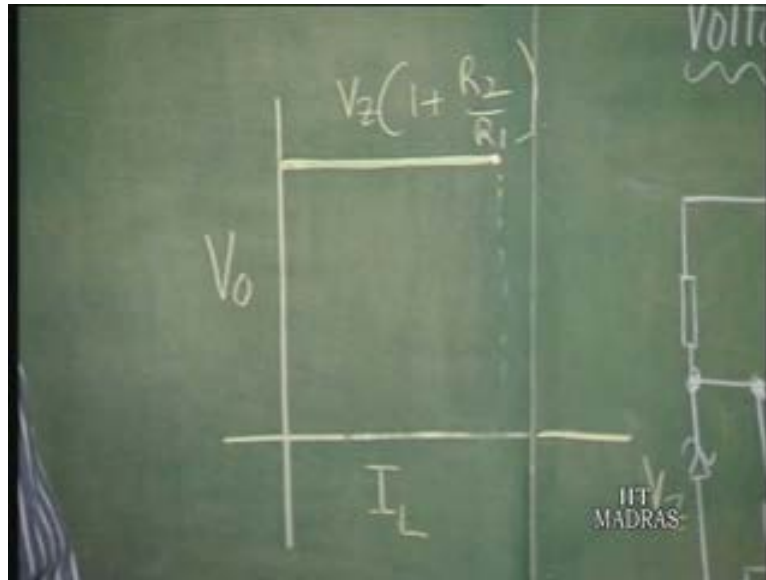
So, in the last class, we had seen that this kind of series pass regulator works very nicely maintaining voltage constant at a value which is V_z in; or depending upon the design, we can make it V_z into $1 + R_1/R_2$.

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It is the external circuit that is put so that this is V_z into $1 + R_2/R_1$. This is the regulated voltage at which it is maintained. Up to what current can it maintain this? This also we had discussed in terms of the ability of this circuit to function.

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But apart from that, suppose it, by accident, gets short circuited. What will happen? Because then, it may not regulate obviously, and forcibly making this zero. So, nothing can help it because voltage has to become equal to zero. It cannot be maintained constant. So, what happens now is this is shorted. This is V_i and this voltage is V_γ .

So here, $V_i - V_\gamma$ by R_c is going to be pumped into this. At best, this current can become equal to, let us say, I_{naught} . So, most of the current which is very high, $V_i - V_\gamma$ by R_c , will be pumped into the base of this and this Beta times that will be too huge a current for this transistor to tolerate. And therefore, this transistor will get destroyed because the current maximum, they get exceeded; or its power maximum... Look at this. The...this is V_i and this is zero. So, the entire voltage is across the transistor, V_i .

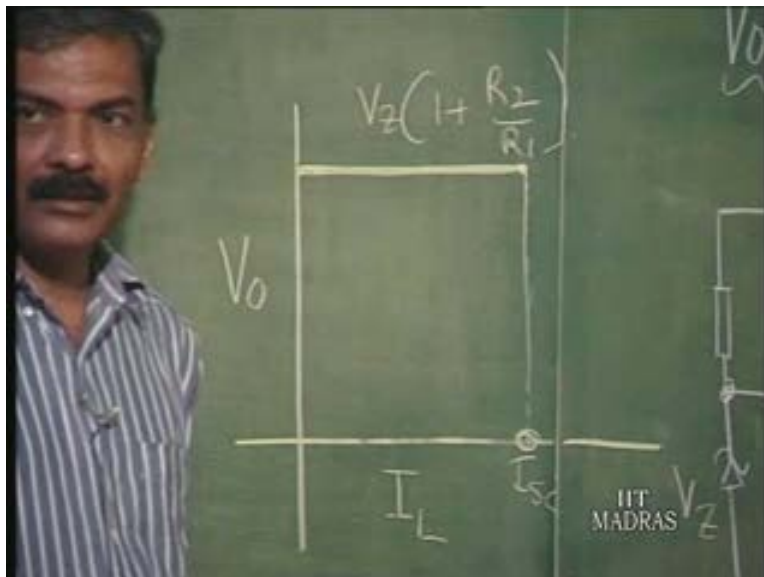
So, the power dissipated is simply V_i into I_i ; and the power dissipated for this transistor when it is not working under this situation may exceed whatever it is when it is working. When it is working, we will see that the voltage across this, it is simply $V_i - V_{naught}$; much less. And it might carry large current. So, since the voltage across it is very small, the power dissipated could be maintained quite small, under limit.

So, this is a very serious thing. This, we should not let it happen. Suppose there is a short circuit. We do not want really the output to be regulated; but we want the transistor to be protected. This is a mistake. We are using a load which is more than what we are permitted to use. So this need not work; but it should not destroy itself. That is the idea behind protection.

So, we will protect it by converting it into something called current source. This is a voltage source. That is why it is able... it delivers whatever current you are trying to demand. It is trying to demand infinite current and therefore this is trying to deliver the maximum possible current it can; that is, trying to get the base drive to itself.

So, this kind of thing is what we have to prevent. That is, current exceeding a limit. Let us say, this is the maximum limit based on, let us call this I_{sc} . Actually, it is not a short circuit current. It is a current that we will evaluate by finding out what is the maximum dissipation that is likely to occur here. So now, if this current is permitted through this transistor, the maximum dissipation in the transistor is going to be simply V_i into I_{sc} that is occurring here, not here.

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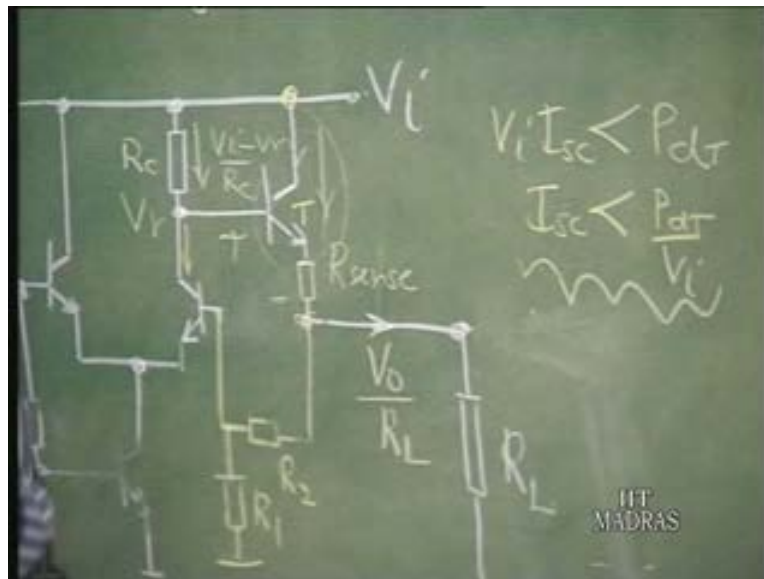
So, based on this, V_i into I_{sc} that should be less than power dissipation of this transistor T, pass transistor T. So, based on this worst case...worst case is V_i ... that is, this current, the lowest value possible is V_i max. When V_i is maximum, power dissipation is maximum. Then this gives you the lowest limit for the maximum current we can permit through the transistor, when it is short circuited, when the regulator is short circuited. So, this is an important rating.

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The image shows a chalkboard with handwritten equations. The first equation is $V_i I_{sc} < P_{dT}$. The second equation is $I_{sc} < \frac{P_{dT}}{V_i}$. Below the second equation, there is a wavy line representing a sine wave, with V_i written above it. In the bottom right corner of the chalkboard, the text "IIT MADRAS" is visible.

Suppose therefore, I want to limit the current to this value. So, I now put...the technique of limiting is by putting a series resistance. But if I put a series resistance and limit, the output resistance is going to increase, because if I want to limit this current to this value, I have to now put a resistance which is pretty high in series with the load which is not good thing because we want the output impedance of the regulator to be low. But I have to find out the current in any case. So this is really called sense resistor. It is there only to sense the current; to tell you what you should do if it exceeds a certain value. So, this is a sense resistor.

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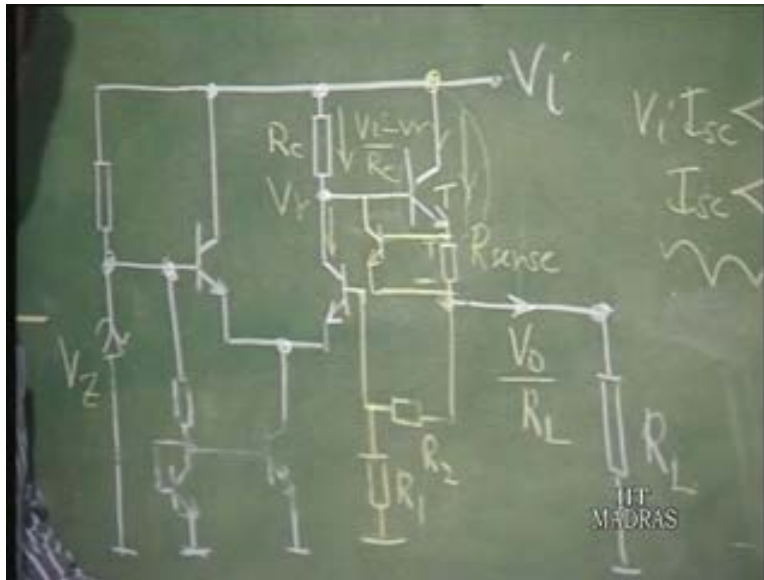


It can be low compared to load resistance. So, the output resistance is kept low. So, this sense resistance will sense the load current here. So, what is the load current? V naught by R_L . So, this V naught by R_L will flow through the sense resistance and if R_L is decreased, this current increases and this voltage increases.

So, what do we do? Normally...suppose there is traffic jam in a road. What does the police do? The traffic police. He will divert the traffic to side roads because a particular road can take only a certain amount of traffic. So, he will start diverting the traffic to other roads and then ultimately it will go to the destination anyway. So, this is the idea here. Why is Z current increasing here when the load is decreased? This current is increasing because the base current is increasing. If we do not let the base current increase, this current cannot increase.

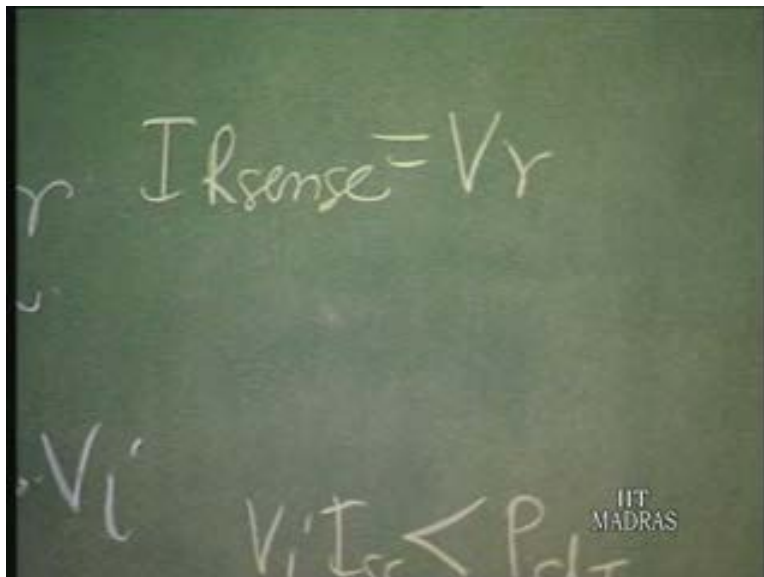
So, what we will do is we will divert the current on to another transistor. This is the protection transistor. This transistor will come into picture only when the current exceeds a certain value.

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So we have this protection transistor getting forward biased because of the current that is flowing through R sense; and when I into R sense, when this becomes equal to V Gamma, the cut-in voltage of the transistor, this transistor starts conducting.

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What will it do? Earlier, the current was simply going into this. This was the current supplied to the base of the series pass transistor. This is simply going there. Now

suddenly, this is conducting and this is saying that I am free, this road is empty. Why are you going to a road which is getting packed with traffic? Why don't you come here? It is almost empty. You can go to the same destination. So, this diverts this current to this. The advantage is this traffic is not amplified. That is because of this. If it has been permitted to go into the base, it will be Beta plus 1 amplified. But here, it will simply come as a diverted traffic on to this road. So, this comes here.

So, what is the current at which this can come into picture? We can evaluate that. That current, I short circuit, is nothing but V Gamma divided by R sense.

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Handwritten equations on a chalkboard:

$$I_{rsense} = V_\gamma$$

$$I_{sc} = \frac{V_\gamma}{R_{sense}}$$

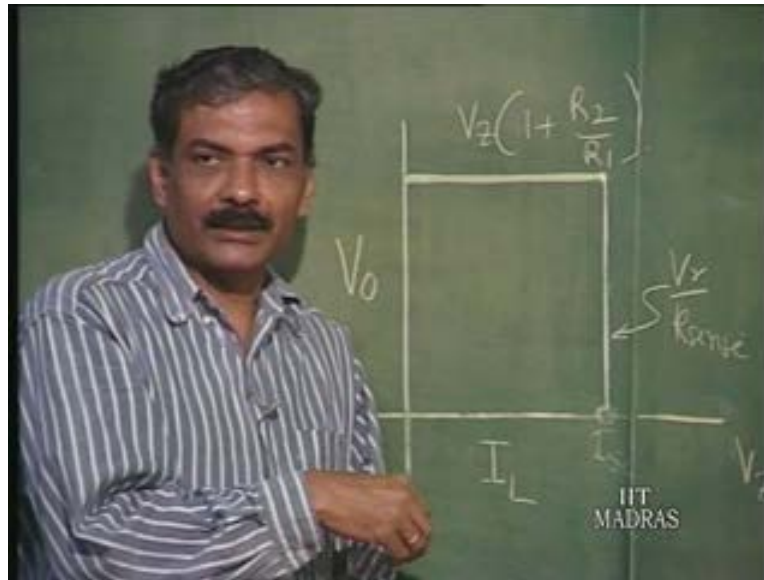
$$V_i I_{sc} < P_{dT}$$

IIT MADRAS

V Gamma is something like point 7, let us say. And I want this R s c, I s c, fixed by this limitation, to be, let us say 1 ampere. Suppose this is 1 ampere. Based on power dissipation maximum criteria, we have fixed it at 1 ampere.

So, I s c is 1 ampere. So, R sense required is point 7 by 1 ampere which is point 7 ohms. This is a resistance which is not normally available to you. You might have to wind it using resistor wires. So, a small resistance you will make and measure it to be exactly point 7. Then, that will limit it to 1 ampere. So, this is the way.

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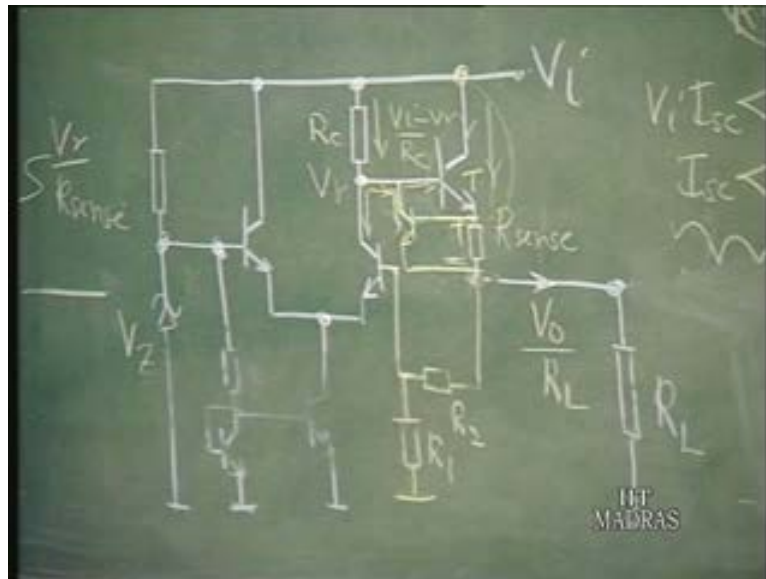
What is the characteristic then? The characteristic is going to be like this. That means after this load, it will become a current source instead of a voltage, constant voltage source. Up to this it was constant voltage source. Here, the current is constant at what? V_γ by R_{sense} . So, voltage can be anything. So, it is...this is the short circuit protection.

So, this is really what we are saying...short circuit...I have to clarify certain things. Short circuit here simply means, in this context is not really your voltage equal to zero. A current exceeding the limited value that is given for this circuit, for this transistor. That load is a short circuit load. So, the moment that resistance or any resistance less than that is put, all such resistances are short circuits for us. So, a protection comes into picture and limits the current at that value.

So, please remember that this is not really the current when voltage is zero. The current when voltage is zero is now limited to V_γ by R_{sense} . That current is the same current at any other voltage, between this and this.

So, it is maintaining constant current of V_{γ} by R sense throughout. So, this is a very important short circuit protection scheme which can be incorporated also in power amplifiers; not only in voltage regulators. In class B power amplifiers or class A power amplifiers, we can incorporate this, so that the accidental short circuit of low output impedance stages is prevented. The hold thing gets converted into a current source.

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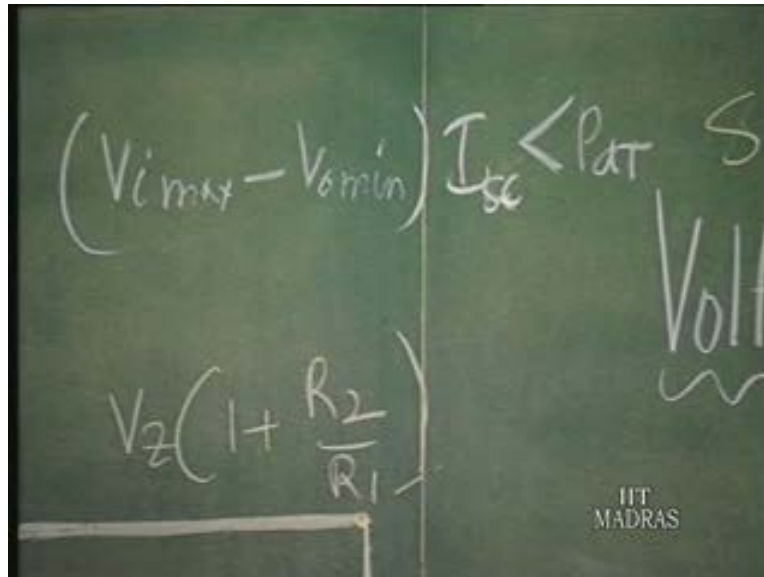
Now, let us see the protection we have rendered for this transistor, pass transistor. At what cost, let us examine it. See, after all, it is not that every day I short circuit the voltage regulator. That is normally an accidental thing.

So, it might happen once in a blue moon and it might remain like that causing lot of dissipation in this transistor, because if this is shorted, lot of dissipation occurs. Until somebody comes and removes it, that will happen. That is why we have to now restrict I_{sc} for this regulator based on the requirement that V_i into I_{sc} should be less than power dissipated in the transistor.

But, that is only for an eventuality, when accidentally we are short circuited. We are... If we are sure that it is not going to be short circuited at all, then we could have taken a I_{sc}

which is higher because that will be based on $V_{i\max}$ minus $V_{\text{naught minimum}}$ into I_{sc} . This should be less than the power dissipated in the transistor.

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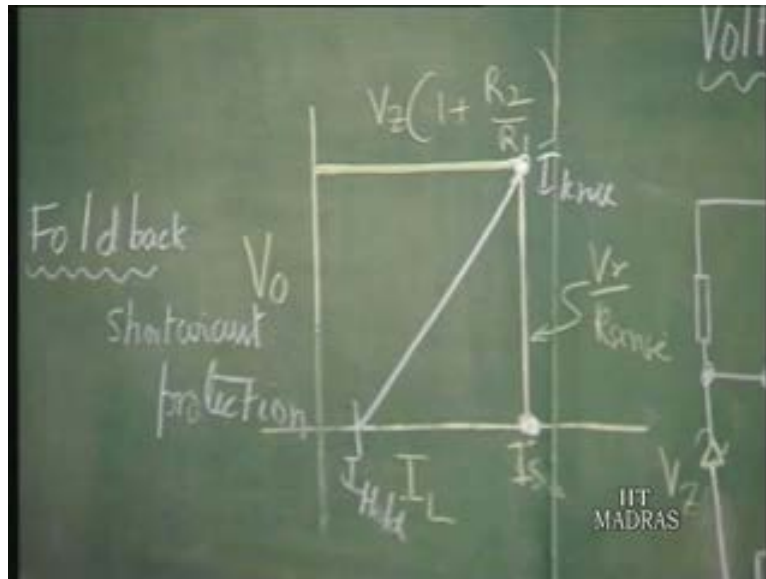
This would have given us an I_{sc} which is much higher than this. That means the regulator can be really made to work over a wider current range than what is now being done.

Why? That is because maximum power dissipation occurs in the transistor at this point; whereas, this is the limiting point of operation at which power dissipated is much less in the transistor. So, this not a good way of protecting the transistor. If it is not working in this region of load, why should I maintain a constant current? Why should I put in an extra effort to maintain current constant? That is the logic in what is called fold back short circuit protection.

So, why not make the current decrease? Why not make the current decrease because any way it is not going to work here? So, why not make the current decrease as the R_L decreases?

So, this is called fold back short circuit protection. Therefore, I have to have here...even when actual...this is the actual short circuit. R_L is zero. So, V_{naught} is zero. At that point, I must have a scheme of maintaining the transistor in this mode. So, this is called I Hold and this is becoming a knee. So, instead of calling it as I_{sc} , I call this current as I_{knee} which was earlier our $I_{\text{short circuit}}$.

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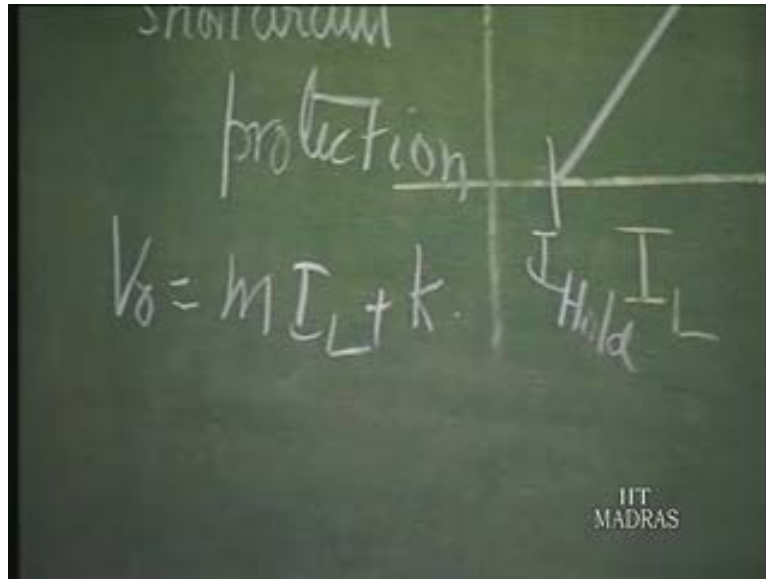


But now, I_{knee} can be much higher for the same rating of the transistor; then $I_{\text{short circuit}}$ because now, we can examine that the power dissipated is going to be lower. Particularly under short circuit situation, it will be pretty low. So, until the short circuit is removed, it can remain in this. So, no harm; particularly in regulators which are not likely to remain attended for long periods of time, this kind of short circuit when it occurs, it might destroy otherwise, the regulators.

So, until somebody comes and realizes that there is some short in the load and removes it, it will remain in this mode. Then it automatically can go back to the regular mode. So, this kind of short circuit protection we can implement. Let us see how. Obviously, this line is nothing but V_{naught} ...this is the y axis...is equal to some m slope into I_L plus

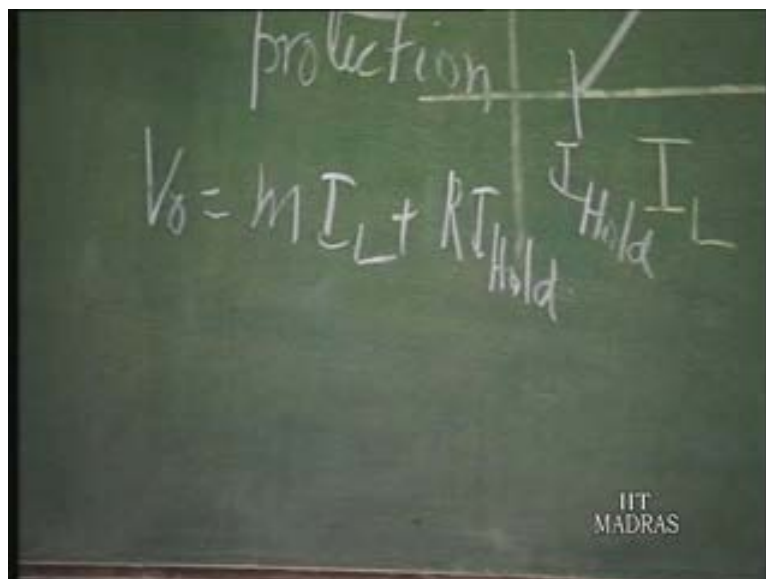
some constant, the K. This is the equation of this line. V naught is of some slope, positive slope and some intersect.

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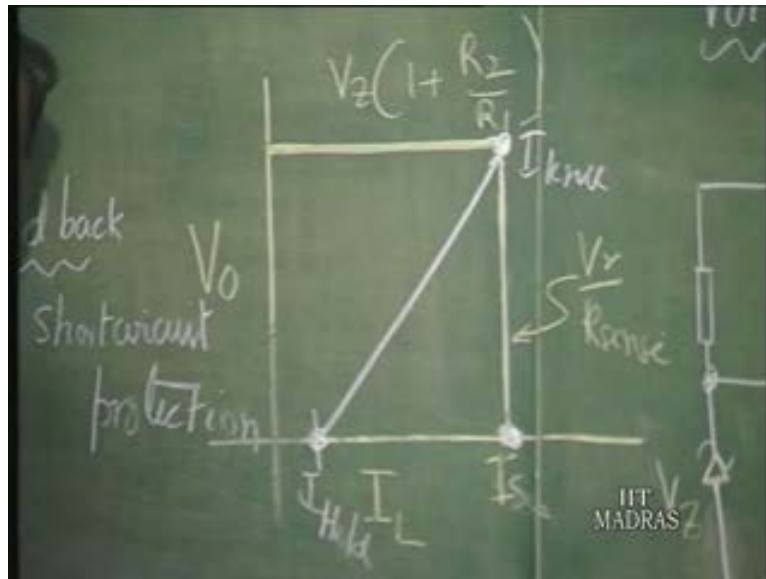
So, the intersect is obviously the...corresponding to I Hold. Some R times I Hold, when I L is equal to zero, V naught is equal to zero. So, this is the kind of equation for the line. We will try to derive this.

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You know this point I Hold. You have decided that there shall be a minimum current, I Hold. We will also see how this I Hold can be decided because we can...we would like to have I Hold as small as possible. What is it that prevents it from becoming zero? It cannot be zero and why is there a limit on I Hold? I knee... at this I knee, the voltage is already known. It is $V_z \left(1 + \frac{R_2}{R_1} \right)$. At this I Hold, voltage is zero.

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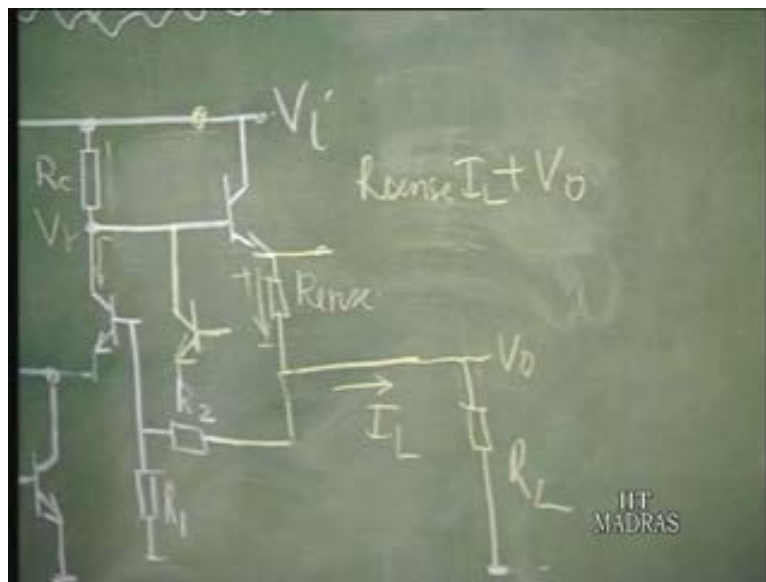


So, given two points, we can always draw a line passing through this. So, let us try to write down the equation later in terms of this scheme which is going to implement this. So, obviously, I had to have the protection scheme working based both on voltage and current, because now I cannot depend only on voltage.

So the sense...voltage as well as current, output voltage as well as current, should be fed into the base emitter junction of a transistor. That is, same principle. To divert the current from this base. So, as far as protective scheme is concerned, it remains the same in its mode of implementation. Only thing is, now we have to bother about sensing both voltage and current. Earlier, we have sensed only current. So, if I now put a resistance here...

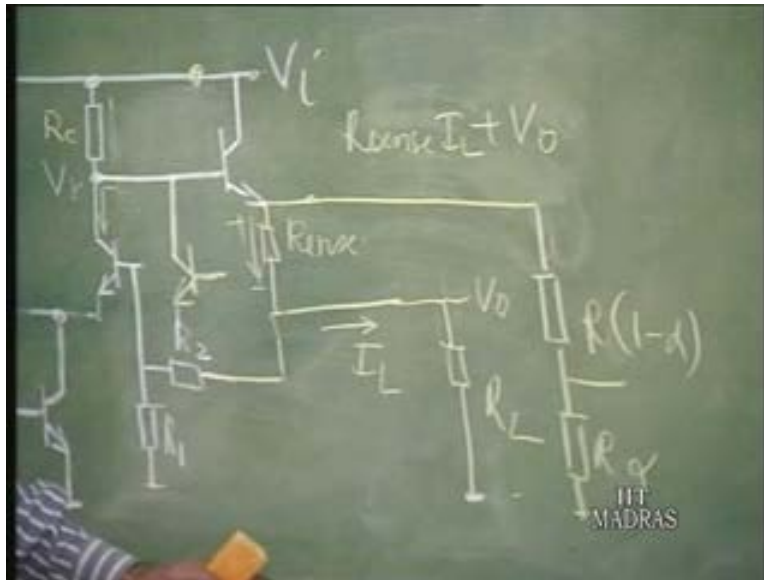
Let us give it enough space there. This is R_L , this is I_L , which is V_{γ} by R_L , V_{γ} by R_L . Now, I will sense the current using R_{sense} . That is, current is sensed. So, the current in this, if it is I , which is very nearly equal to I_L . So, R_{sense} into I_L . I am ignoring this small current here. R_{sense} into I_L plus V_{γ} . This potential here at the emitter point is R_{sense} into I_L plus V_{γ} . So, it gives us information both about output voltage and current, if I take this voltage; but that may be pretty high value. I want only V_{γ} .

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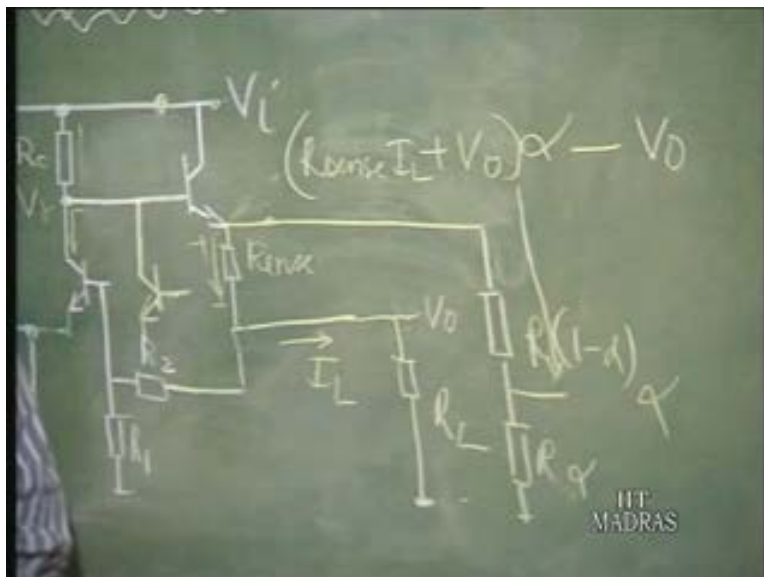
So, I take only a portion of that voltage. Let us put this as R_a and R_b , an attenuator. We will therefore put it, put this as R into α ; R into $1 - \alpha$. These are two resistances. What matters is the ratio.

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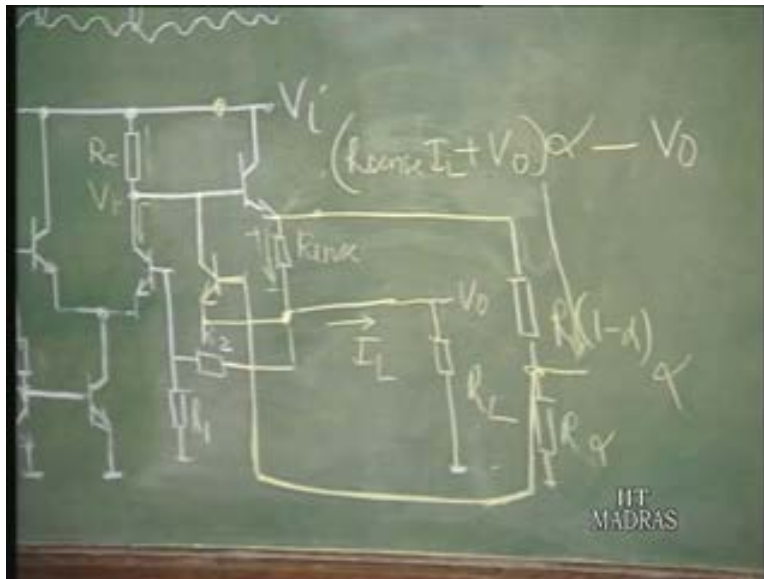
So, the voltage appearing here is going to be this whole thing. This is the voltage here. That into Alpha; that will appear here. Alpha R by Alpha R plus R into 1 minus Alpha which is R itself. So, Alpha... So, the voltage here is Alpha times this. This is the voltage here. That also may be too high a value, minus V_{be} . So now, I have two ways of making the voltage pretty small. Alpha is chosen such that this large voltage is set to a small value, and I subtract V_{be} .

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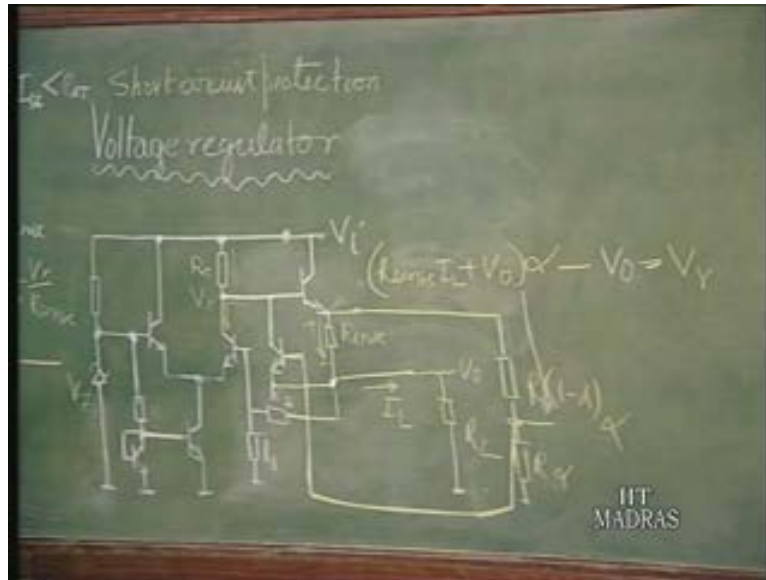
That is because between base and emitter, you are applying some potentials of the protective transistor, transistor which is coming to protect this whole thing. So, if I connect it that way now... So, what is the way? This base is connected to this point. This way. Let us therefore connect it there and emitter is connected to V_{naught} . So, the base potential is this.

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Now, this should be equal to what? V_{γ} , because that is between the base and emitter of the junction. Now this equation, if you say, is an equation containing both V_{naught} and I_L . So, this equation of a line...and we have to make it pass through these two points.

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So, we can apply the limits to these two points and we get the equation of the line. So, if that is the case, then you can now see the two variables R sense and α . Why two variables are necessary here? Because it has to go through two points here.

So, by properly selecting α and R sense, I can make it pass through two points. So this, you can again verify. I_L Hold comes into picture when V_{naught} is zero. So, you can realize why V_{naught} is put this way so that it gets subtracted. Ultimately, there should be some current so that this equation gets satisfied. So, R sense into I Hold, I_L Hold into α - that happens when V_{naught} is equal to zero. That should be also equal to V_{γ} . This is one equation that is making it pass through this point.

The other point is R sense into I knee. That is the other point, plus V_{naught} regulated. V_{naught} regulated actually is V_z into $1 + \frac{R_2}{R_1}$ which is known to us. V_{naught} regulated, minus...this into α minus V_{naught} regulated is equal to V_{γ} . This is the other equation.

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$$\begin{aligned} & (R_{sense} I_{hold} + V_{or}) \alpha - V_{or} = V_{\gamma} \\ & R_{sense} I_{hold} \alpha = V_{\gamma} \\ & (R_{sense} I_L + V_o) \alpha - V_o = V_{\gamma} \end{aligned}$$

So, that will now make it pass through this point. So, you can now find out from these two equations, two unknowns which are R_{sense} and α . So, this completes the design.

Now you can see that this current, you cannot make it zero actually. Hold current - you cannot make it zero because this equation has to be valued. I make Hold smaller and smaller. α is less than 1. As I make I_{hold} smaller and smaller, R_{sense} will have to be larger and larger. What is the problem, you might ask. Of course, R_{sense} is going to be larger and larger in order to satisfy this equation also. But, when it is not under any sort of serious threat of short circuit, this R_{sense} will come as output impedance because this protection scheme is not functional. This whole thing is off - this transistor is off, this transistor is off.

But, R_{sense} still comes into picture. So, there will be a drop, DC drop in the R_{sense} . If there is a DC drop in the R_{sense} , then you can see, $V_{i\ minimum}$ will get higher and higher because this is V_{naught} , this is $V_{naught} + I_L \text{ into } R_{sense}$, when it is working also. And then, V_{γ} and then the drop across this. Earlier, without this, it was simply $V_{naught} + V_{\gamma}$ and some drop across this, which is small.

So now, it is going to be increased. So, the V_i minimum up to which it can work will go up. The limit will go up. So, that is the problem or what is called as V_i minus V_{naught} minimum will increase. So, this is the disadvantage of making I_{Hold} smaller and smaller. So, do not be too greedy. You just make it lower such that the power dissipation maximum gets shifted towards this side.

It was occurring here earlier. Now, it keeps on getting shifted and make it fall outside here, so that power dissipation maximum occurs at I_{knee} . How do you do it? We can do that very simply. What is the power dissipated at in this region? That we will find out. The power dissipated in the transistor is going to be V_i minus V_{naught} into I_L . This is the power dissipated in the transistor. So, this is equal to V_i minus V_{naught} into I_L .

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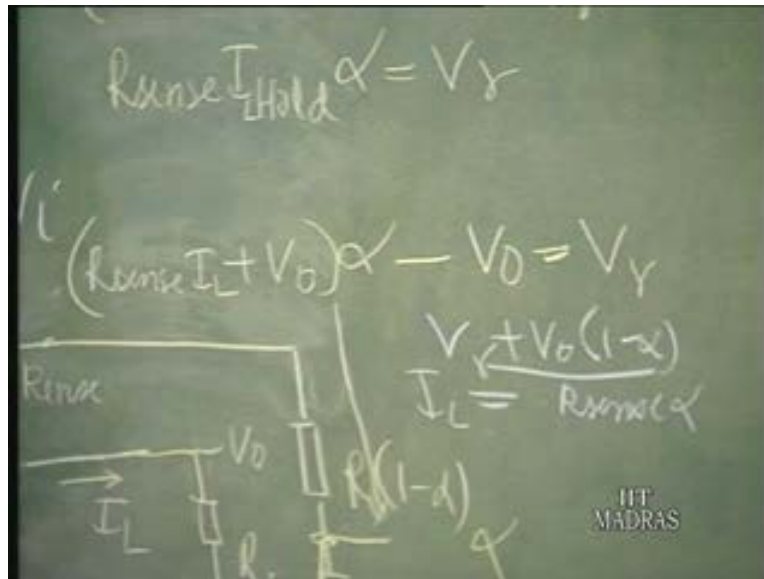
$$P_d = (V_i - V_o) I_L$$

$$= (V_i - V_o)$$

You can actually put instead of I_L , that equation, because in this region, that equation is valid, equation of the line. So, instead of I_L , you can eliminate one variable. This... these are two variables: V_{naught} and I_L . Eliminate one variable using that equation. So, one way is it is going to be $V_{\Gamma} + V_{naught}$. This is going to be $V_{\Gamma} + V_{naught}$ equal to... Then, into $1 - \alpha$.

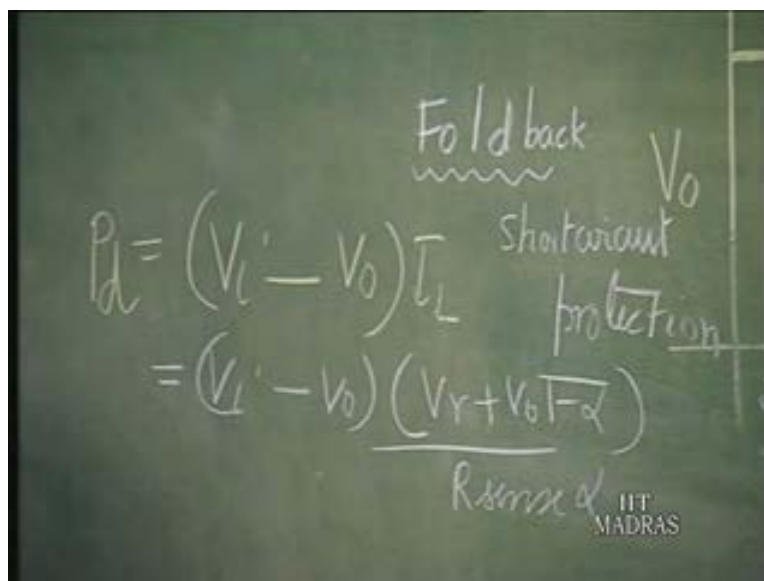
V naught into Alpha minus 1 here. So, when it goes that side, V naught into 1 minus Alpha. That divided by R sense into Alpha is equal to I L, from this equation.

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So, substitute that. V Gamma, Alpha divided by... So, you can get here this fact that it is a quadratic equation in V naught.

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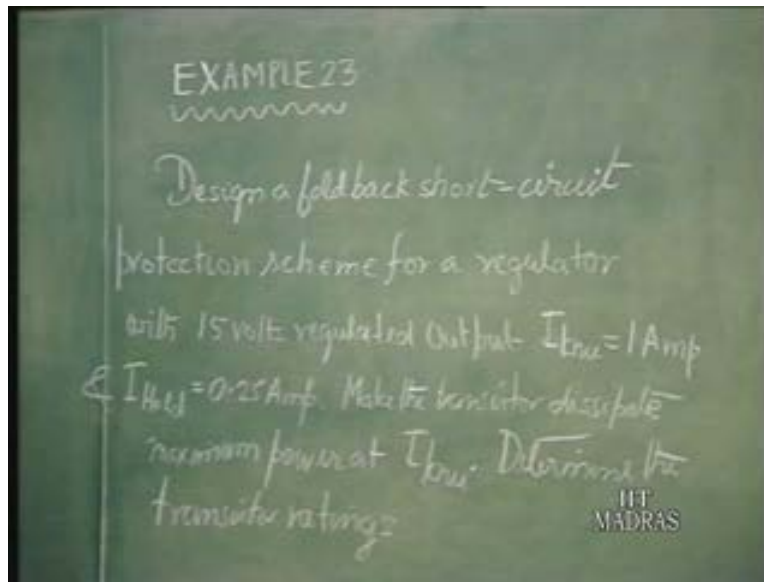


You differentiate this because you want to make ΔP_d by ΔV_{naught} equal to zero. So, you differentiate this and equate it to zero. That will be the V_{naught} . That equation will give you a V_{naught} at which power maximum is going to occur. If that V_{naught} falls outside this, then it is of no consequence because this line will go on like this. If it falls at this point, then the power dissipation maximum can be made to fall here. So, this is one way.

Otherwise, you can find that intermediate point there will be some place where power dissipation maximum is going to occur. I think this particular thing will sort out by working out a specific design problem. So, this way, we will be able to design voltage regulators which are quite efficient and the protection circuitry is not really sort of inefficient. Earlier, protection circuitry was alright but it was not efficient. So, this foldback short circuit protection is commonly employed in all such situations where one is likely not to attend to the short circuit load for long time.

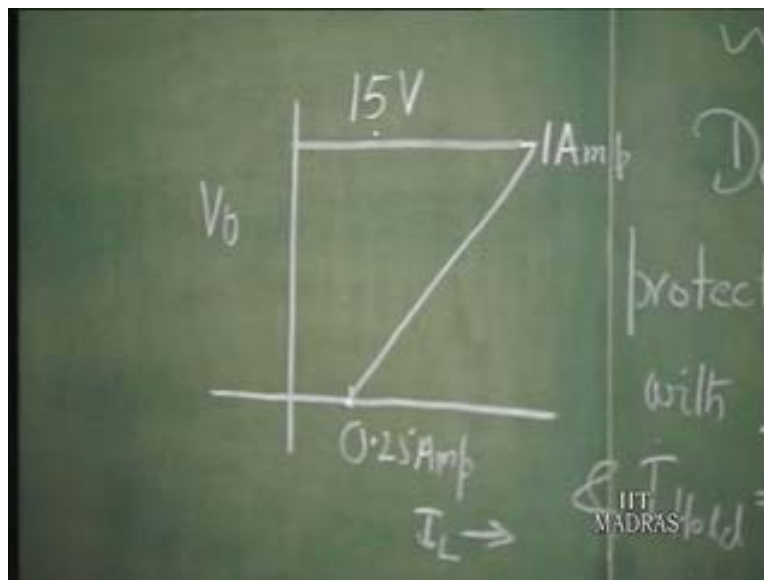
Now we will work out an example in order to understand the foldback short circuit protection. Example 23. Design a fold back short circuit protection scheme for a regulator with 15 volts output, regulated output. I_{knee} is equal to 1 ampere. I_{Hold} is equal to point 25 ampere. Make the transistor dissipate maximum power at I_{knee} . Determine the transistor ratings.

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Now, it is given that this is 15 volts regulated output. V current is 1 ampere. This is point 25 ampere, hold current.

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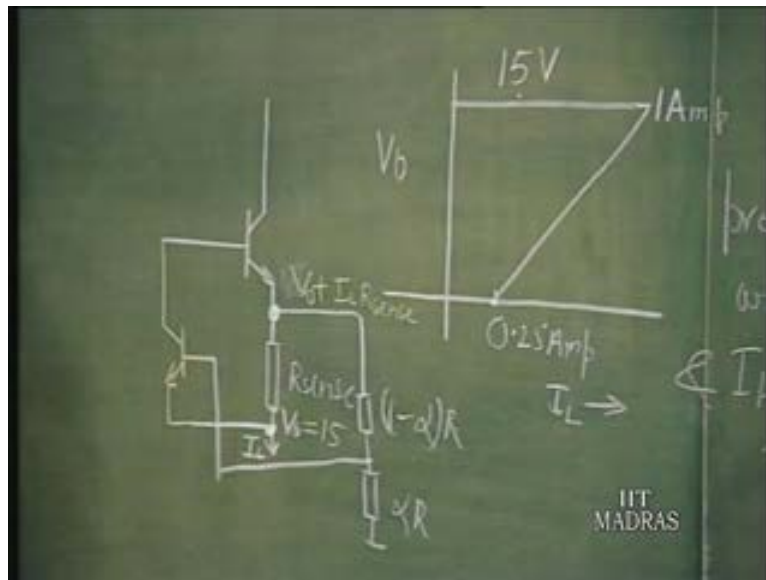


Now, we have seen that the transistor that is to be used, power transistor to be used, this will have a protection scheme, the protective transistor. We will have R sense in series with this. Then, we will have the attenuation network Alpha R, 1 minus Alpha R, and this

point is going to be taken here and this emitter point is going to V_{naught} ; and here of course, we are drawing the current I_L . So, this is the complete short circuit protection scheme using foldback.

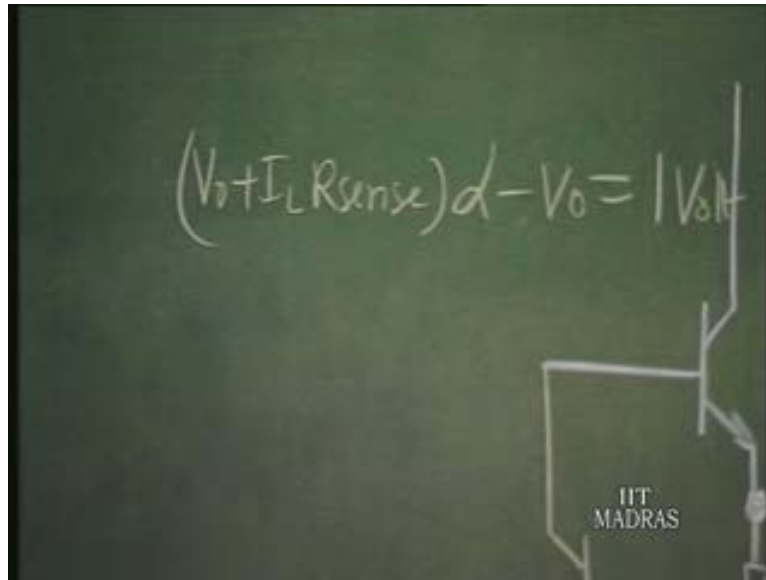
We have here this voltage, as in this case, we said this will be equal to 15 volts. So, this is 15 volts plus I_L into R_{sense} . So, basically this is V_{naught} plus I_L into R_{sense} .

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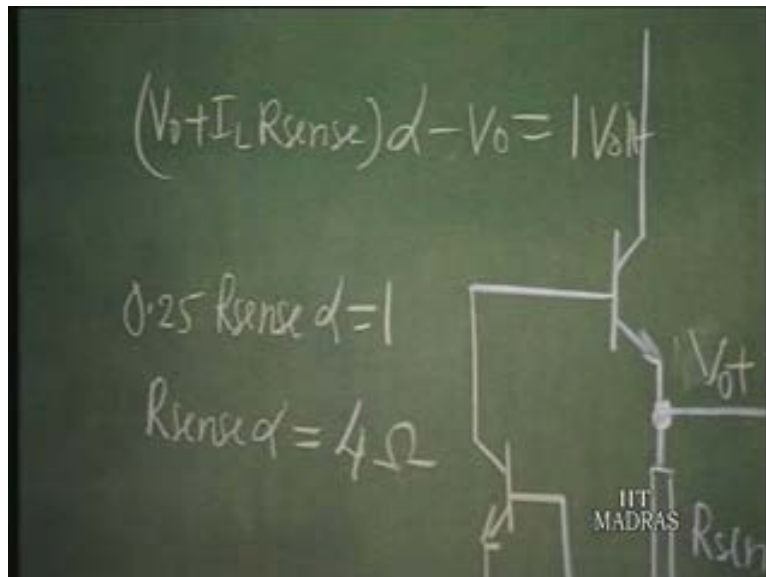
So, α times that - V_{naught} plus I_L into R_{sense} into α minus V_{naught} is equal to V_{BE} . This, we will assume for currents of the order of 1 ampere or so as 1 volt, 1 volt. So, this is the equation of this line now, which is going to satisfy these two points. So, we will substitute this value so that this line is well defined.

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When V_{naught} is zero, the I_{Hold} is point 25. So, I_L is point 25. R_{sense} to be found out, into Alpha; this is equal to 1 volt. So, R_{sense} into Alpha is equal to 4 ohms. 1 by point 25 which is 4 ohms. This is determined from this hold current.

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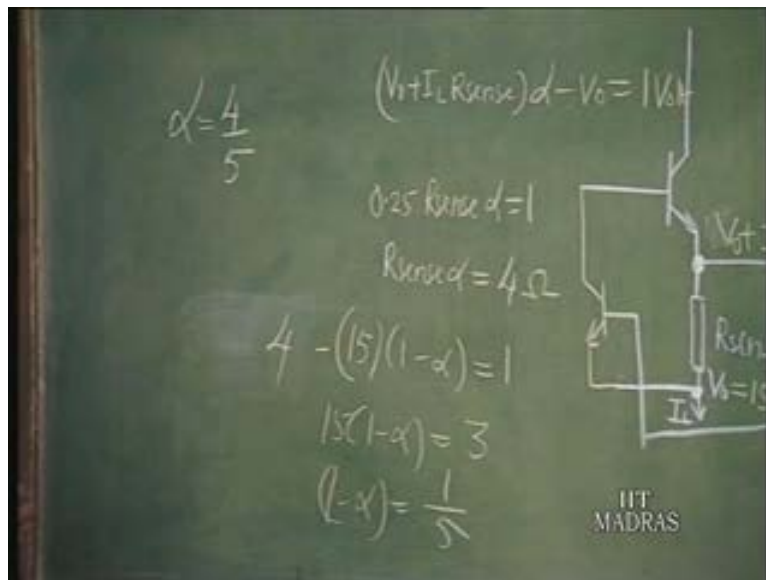


Then... That you can see here that the lower the I_{Hold} , larger will be the R_{sense} into Alpha. So, one thing you we have to notice is that with 1 ampere current and 15 volts, the

load resistance itself is going to be 15 ohms; the lowest value of load resistance - 15 ohms. So, and this is as much as now 4 ohms. So, if we had selected a I Hold lower, this would be, may be, quite comparable to the load resistance. This is the disadvantage of actually taking hold current lower and lower.

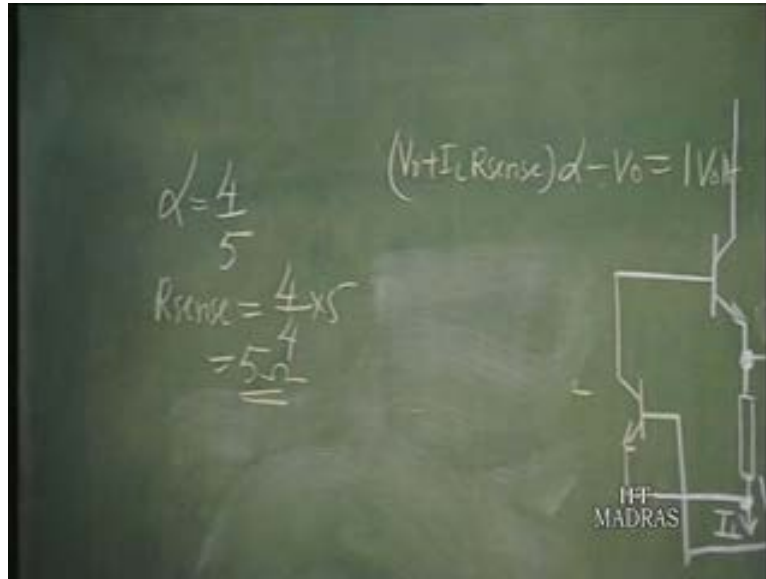
So next, V_{ce} is 15 volts when it is, into $1 - \alpha$ minus... That is going to occur when I_L is 1 ampere. So, 1 into R_{sense} into α , 1 into R_{sense} into α . R_{sense} into α has already been determined as 4 . So 4 minus 15 into $1 - \alpha$. This is equal to again 1 volt. So, 15 into $1 - \alpha$ is equal to 3 . So, $1 - \alpha$ is equal to 1 by 5 . α is equal to 4 by 5 . Is it clear? α is equal to 4 by 5 ; $1 - \alpha$ is equal to this.

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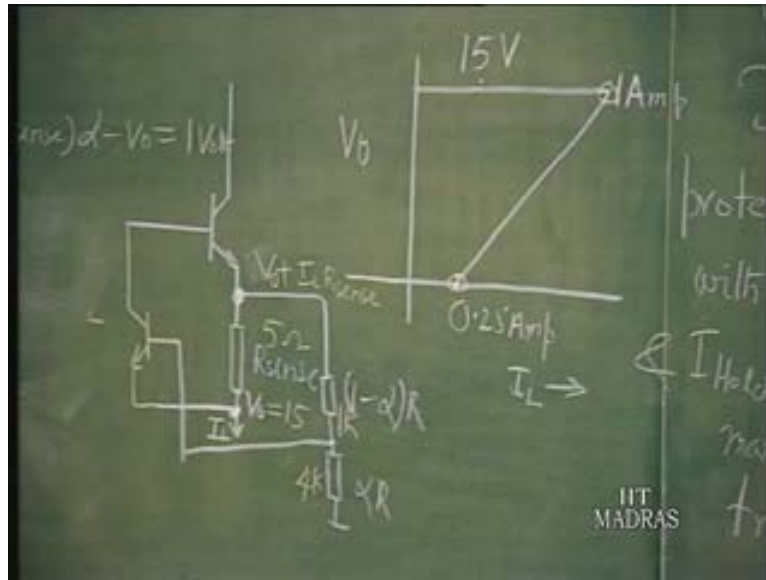
So, we can find out now R sense. Just see here. It is going to be equal to 4 by Alpha - 5 ohms.

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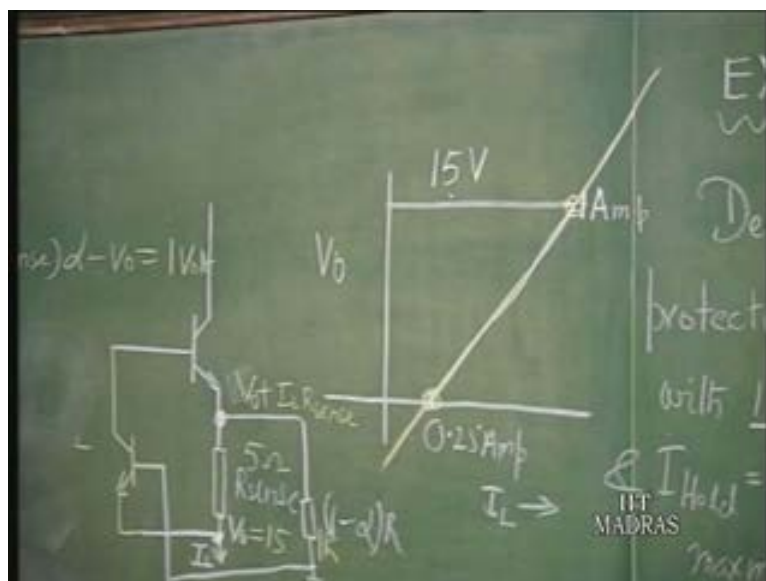
So, we have designed our circuit here as Alpha is equal to 4 by 5. So, may be, this is equal to 4 K and this is equal to 1 K and R sense is equal to 5 ohms. So, the design of the foldback short circuit protection scheme is over; except now, where to take care of power dissipation possibilities? Let us now work towards that.

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This is the line that is going to define this now. This is V_{be} . We do not know what it is; into $1 - \alpha$. That is $1/5$. That into I_L into R_{sense} into α . I_L is a variable. R_{sense} into α was 4 . So, this is equal to 1 volt. This is the equation of this line. Please remember, this line may extend like this. This is the equation of the line, passing through these two points.

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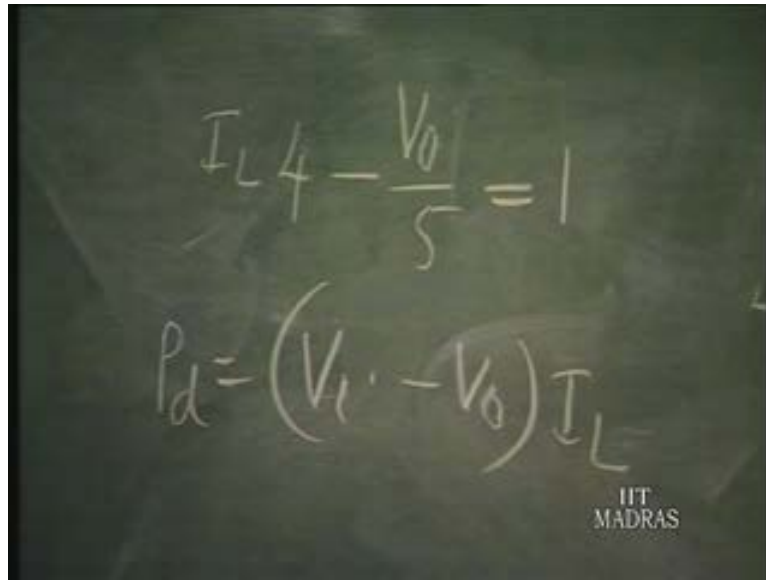
So, this defines this line.

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Therefore, suppose I_L and V_{naught} vary in this line. Then, what is the dissipation maximum, power dissipation maximum in my transistor, which is getting V_i minus V_{naught} as its voltage and I_L as the current? So, V_i minus V_{naught} as its voltage and I_L as the current. This is the power dissipation in the transistor. We would like to maximize this and set the limit at I_{knee} for a specific value of this.

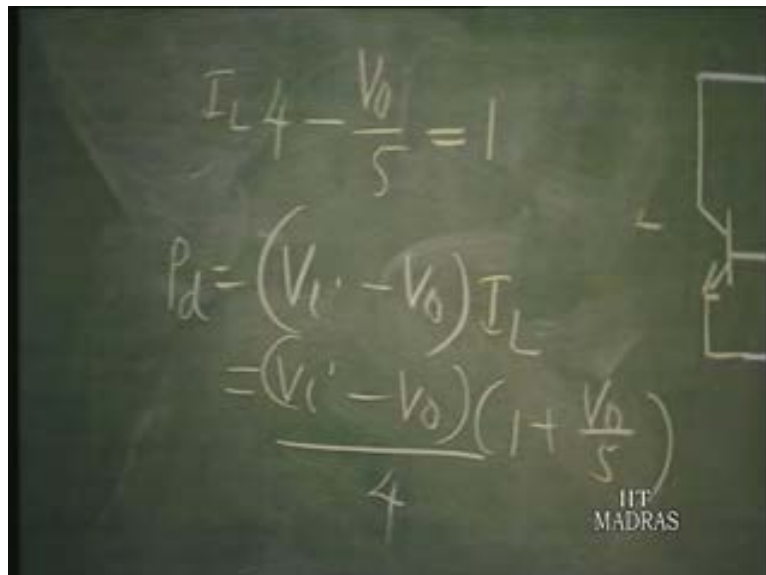
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$$I_L \left(4 - \frac{V_0}{5}\right) = 1$$
$$P_d = (V_i - V_0) I_L$$

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So, when will that take place? For what value of V_i will it take place? If V_{naught} gets fixed, because I_L and V_{naught} get fixed at I_{knee} . So, this is equal to V_i minus V_{naught} . I_L is equal to $1 + V_{naught} / 5$ divided by 4. So, we will now evaluate this.

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$$I_L \left(4 - \frac{V_0}{5}\right) = 1$$
$$P_d = (V_i - V_0) I_L$$
$$= \frac{(V_i - V_0) \left(1 + \frac{V_0}{5}\right)}{4}$$

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This is V_i minus V_{naught} plus V_i into V_{naught} by 5 plus, minus V_{naught} square by 5. Yes. That divided by 4.

So, we find out ΔP_d by ΔV_{naught} . V_{naught} is the variable in this line. Please remember. Where will the maximum occur? That will be happening when, let us say, this becomes 2 by 5 into V_{naught} , 2 by 5 into V_{naught} . When that becomes equal to V_i by 5 minus 1. After differentiating this, this becomes 2 by 5 into V_{naught} , this side. This is V_i by 5 minus 1. So, this is the condition when this becomes equal to zero.

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The image shows a chalkboard with the following handwritten equations:

$$P_d = \frac{V_i - V_0 + \frac{V_i V_0}{5} - \frac{V_0^2}{5}}{4}$$

$$\frac{\partial P_d}{\partial V_0} = 0 \quad \frac{2}{5} V_0 = \frac{V_i}{5} - 1$$

$$I_L 4 - \frac{V_0}{5} = 1$$

In the bottom right corner of the chalkboard, there is a logo for IIT MADRAS.

Now, we want this equation...of this condition to be satisfied at a specific value of V_{naught} . What is the value of V_i ? So, this is going to be satisfied at V_{naught} equal to 15 volts, 15 volts, if V_i by 5 is equal to this. That means 6 plus 1 – 7 for V_i equal to 35 volts.

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$$P_d = \frac{V_i^2 - 2V_i V_o + V_o^2}{4}$$

$$\frac{\partial P_d}{\partial V_o} = 0 \quad \frac{2}{5} V_o = \frac{V_i}{5} - 1$$

$$I_L \left(4 - \frac{V_o}{5} \right) = 1 \quad \frac{15 \times 2}{5} = \frac{V_i}{5}$$

$$V_i = 35V$$

$$P_d = (V_i - V_o) I_L$$

So, for V_i equal to 35 volts, this is going to be satisfied. That at V_o equal to, in this line, at V_o equal to 15; that is where we want. We could have located it here or here or here. We want purposely, this to take place here. If you want it to locate here, V_i should have been still higher. So, for V_i equal to 35 volts, this gets satisfied and we can find out the power dissipation maximum there, from this expression here.

V_i is 35. V_o is 15. V_i is 35. V_o is 15, plus... V_i is 35 into 15 by 5 minus V_o squared 15 squared divided by 5. That whole thing divided by 4 is the maximum power dissipated. So, this is important answer. So, this is equal to... this is 20 plus 105 minus 45. So, 125 minus 45 which is 80 divided by 4. So, this corresponds to 20 watts.

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The image shows a chalkboard with handwritten mathematical work. At the top, there is a faint equation: $V_L - V_0 + \frac{1}{5} = \frac{5}{3}$. Below it, the power dissipation P_d is calculated as follows:

$$P_d = \frac{20 + 105 - 45}{4} = 20 \text{ W}$$

Below this, there is another equation: $I_L \cdot 4 - \frac{V_0}{5} = 1$. To the right of this, there is a calculation: $1 + \frac{15 \times 2}{5} = \frac{V_0}{5}$. In the bottom right corner of the chalkboard, the text "IIT MADRAS" is visible.

That means, if that happens, the maximum power dissipated at this knee is going to be 20 watts. That means the transistor that I had to select, its rating should be greater than 20 watts. So, this is an important criteria for the design.

So, power dissipated in the transistor, that power dissipation rating should be greater than 20 watts. If P_d max rating... The current obviously should be greater than 1 ampere. Current maximum greater than 1 ampere. Power maximum should be greater than 20 watts.

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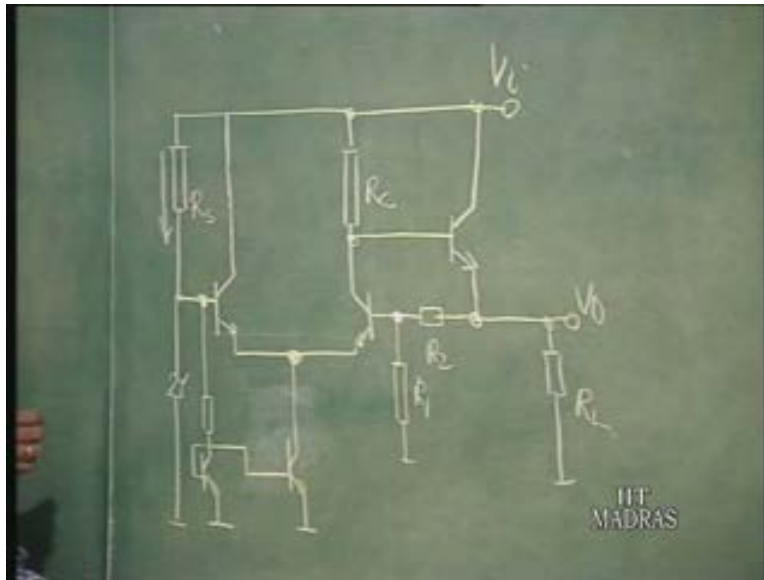


These are the important ratings for the power transistor. That is the pass transistor. So, you will see that this has resulted in a considerable amount of drop in the so-called this resistor. See... Let us now find out. This is 15 volts; and when the current is 1 ampere, there will be a drop of 5 volts here.

So, this is 20 volts and there is 1 volt. 21 volts. That means V_i minimum has to be greater than 21 volts. V_i minimum has to be greater than 21 volts and that increases as R_{sense} increases. So, even though your circuit is going to be pretty efficient in terms of protection scheme, you are dissipating lot of unnecessary power in this because the differential voltage keeps increasing as R_{sense} increases. This is the main disadvantage of making this lower and lower.

Now, I would like to tell you something about some aspects of improving the design of the voltage regulator. We just mentioned that as V_i changes, the current in this is not changing. When this current here changes, V_z also changes slightly. Since output voltage is V_z into $1 + R_2$ over R_1 that also changes. That is what is called as line regulation.

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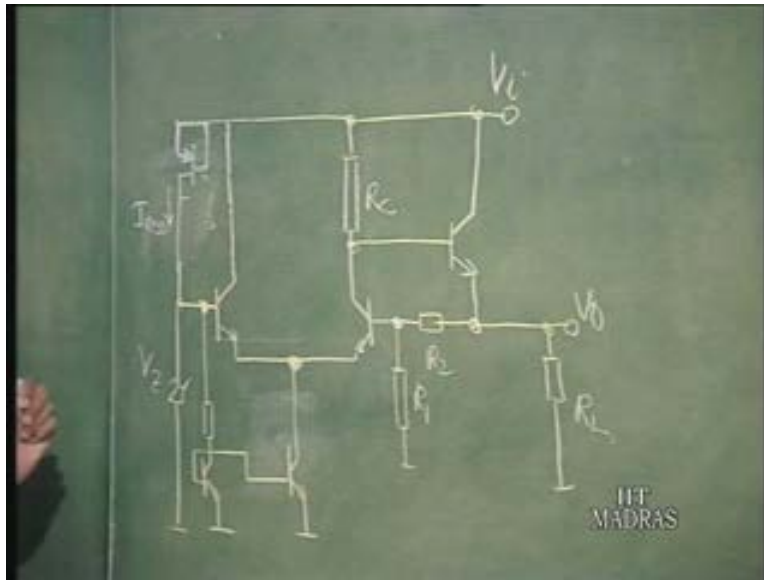


How to improve line regulation? This also influences in what is called ripple rejection because as ripple will appear at V_i and that V_i will cause change in current in this, that will cause a change in voltage normally; and that change in voltage will also come as $1 + \frac{R_2}{R_1}$ at the output. So, both ripple rejection and line regulation factor can be improved if we make the current here constant. One way is to put a current source.

So, one such current source is simply a FET current source where, say a field effect transistor with V_{GS} equal to zero. So, current is going to be $I_{D,s}$. Only thing is, the voltage input has to be greater than V_z by a factor of V_p so that it is beyond being pinch off, so that it enters the current saturation region. So, V_i minimum should be greater than V_z plus V_p coming from this side. All other factors also fix up V_i minimum in their own fashion. We have seen this earlier.

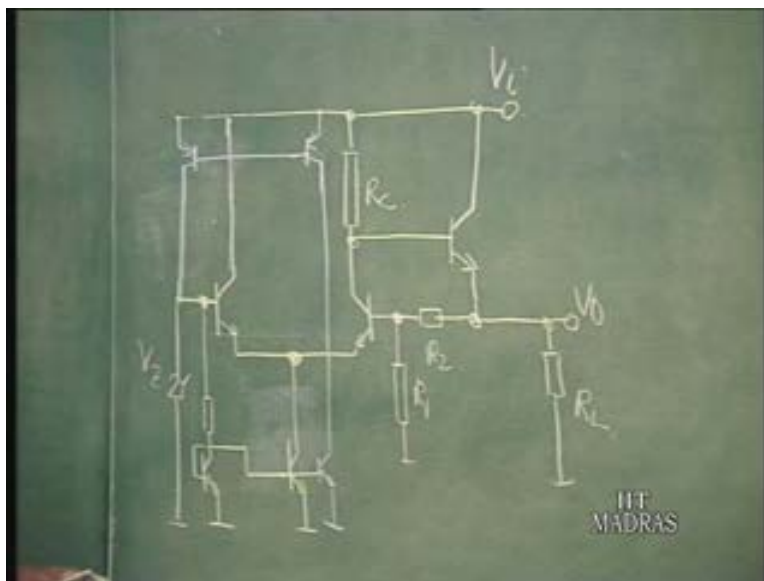
So, this also has to be taken into consideration. The lowest of the... the highest of the V_i minimum is what should be ultimately chosen for the circuit. Now, this is one way.

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Another way is...After all, this is...if this is a Zener, this current is a constant. This current is a constant. This is a current mirror; and therefore, this current can be really used for deriving some kind of current source here like this, let us say. This is a constant current. And put a diode and reflect the same current mirror here. So, this is one way.

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This is a current mirror. This is a constant current. This current is constant. This is another current mirror using, actually again, transistor here. But whole trouble is when you start, V_i may be zero. If V_i is zero, this Zener won't break down. If Zener does not break down this current will not get generated. This bias will not... So, there is starting problem with this circuit. So for that, you can actually use what is called a starting circuit.

So, we will have some R_1 and R_2 or R_a and R_b we will put. R_a plus R_a by R_b is a voltage which is less than the Zener voltage so that, as soon as you switch on, that voltage comes here. This diode conducts because there is nothing here. This will pump a current into the transistor and bias this. And this will bias this and this will bias this and this gets bias current here. Then it causes breakdown of the Zener. Once breakdown of the Zener is caused, this V_z is going to be at a potential which is lower, let us say, than this.

So, we have to have R_a by R_a plus R_b into, what is that? V_i , at any time less than V_z . Then, this gets automatically reverse biased and it goes out of it.

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So, this kind of thing improves drastically the line regulation and ripple rejection. So, this is the circuit that is quite commonly used for improving the voltage regulator in...even in the IC, this kind of structure is used.