High Speed Devices and Circuit

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Lecture – 28

MESFET – Velocity Overshoot Effects And Self Aligned MESFET – SAINT

We have been discussing the velocity overshoot effect and the self-aligned MESFET. It is called self SAINT.

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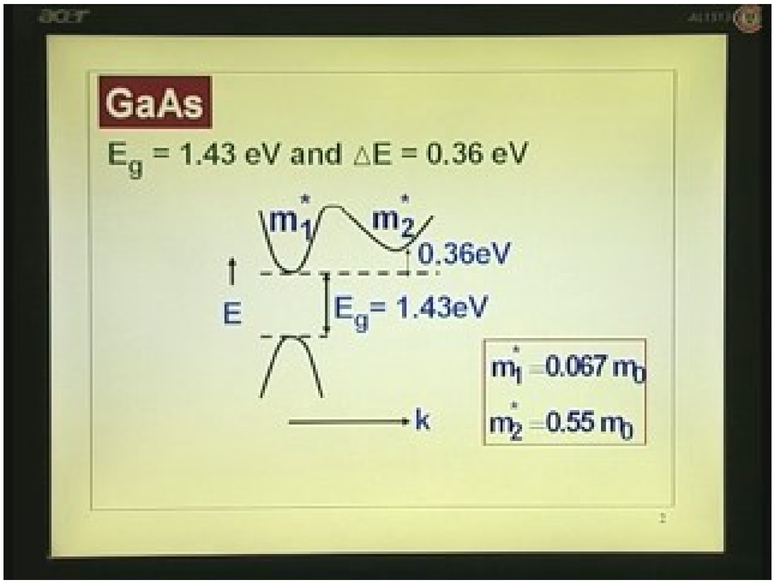

GaAs

$E_g = 1.43$ eV and $\Delta E = 0.36$ eV

$m_1^* = 0.067\ m_0$

$m_2^* = 0.55\ m_0$

Now few things I want to remark, just reviewing what we did last time. We took a look at the energy band diagram, EK diagram and then said that the velocity field characteristics that you get, E is due to the transfer here to here. Also we said that the energy required transferring from here to here, from the lower valley to upper valley. It depends upon the semi conductor that you are using. For example, if you take gallium arsenide, the gap between the upper valley and lower valley, energy gap is 0.36 electron volts and this is 1.43 electron volts. What matters is this gap. Higher this gap, between the upper valley and lower valley, more is the energy required to transfer electrons, more is the electric field. The transfer of electrons takes place at higher fields. That is seen when you compare gallium arsenide and indium phosphate.

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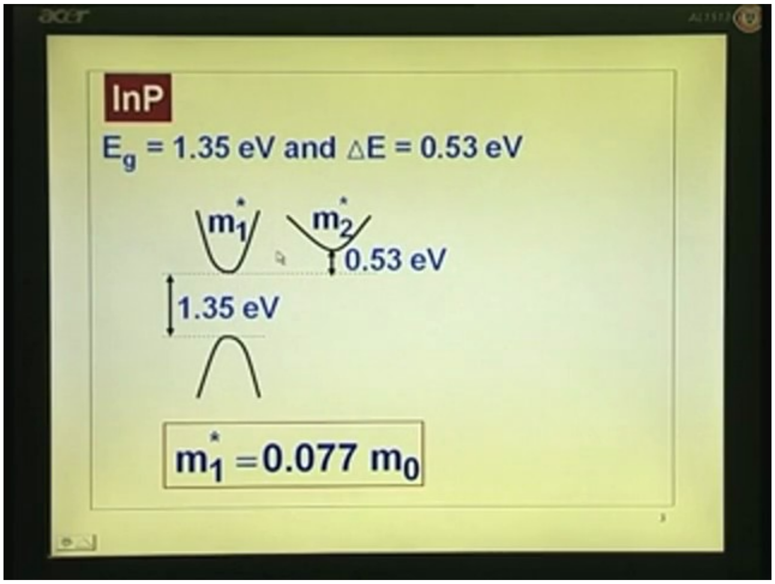

InP

$E_g = 1.35$ eV and $\Delta E = 0.53$ eV

$\boxed{m_1^* = 0.077\ m_0}$

Indium phosphate band gap is slightly smaller, but this gap is larger

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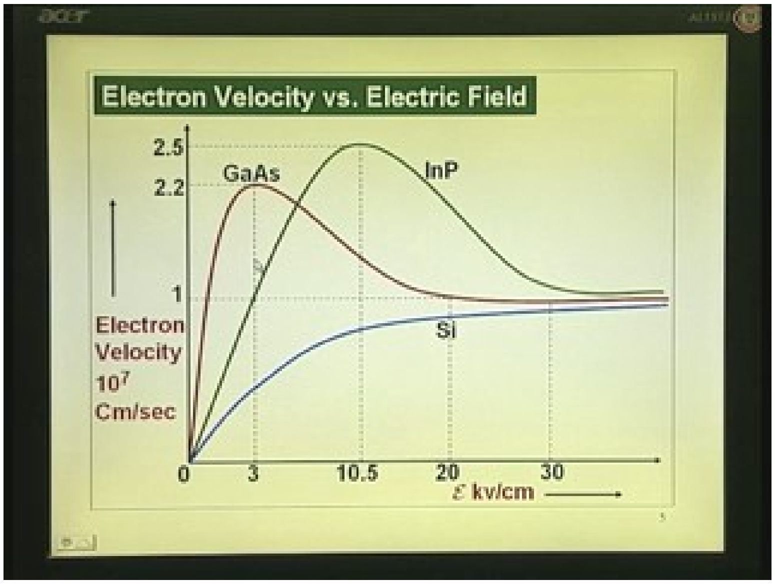

Electron Velocity vs. Electric Field

In fact, I will just skip one of this; as a result, you get the electron velocity, steady state velocity versus electric field in this fashion. You can see that the transfer is at 3kv per centimeter, for gallium arsenide. From that onwards the electrons find themselves in the upper valley. More and more go into the upper valley where the effective mass is larger so its velocity falls. When a complete transfer takes place the velocity is governed by the upper valley. Now you can see indium phosphate, this makes lot of difference for the material with the electrical properties of the two materials. Indium phosphate band gap is 1.43 but the delta E, gap between that upper valley and lower valley is 0.53 as compared to 0.36 here. The transfer takes place at 10.5 kilo volts per centimeter. Transfer from the lower valley to upper valley that means higher field. You can call this as the electric field corresponding to peak velocity, we refer it as E peak or transition electric field and that is almost over three times the field here. Also notice saturation velocity is not much different, nothing much to boost off. You cannot say gallium arsenide has got very much different saturation velocity than the silicon, but the point that we have to notice is, there is a wide range of electric field over which the fields are high.

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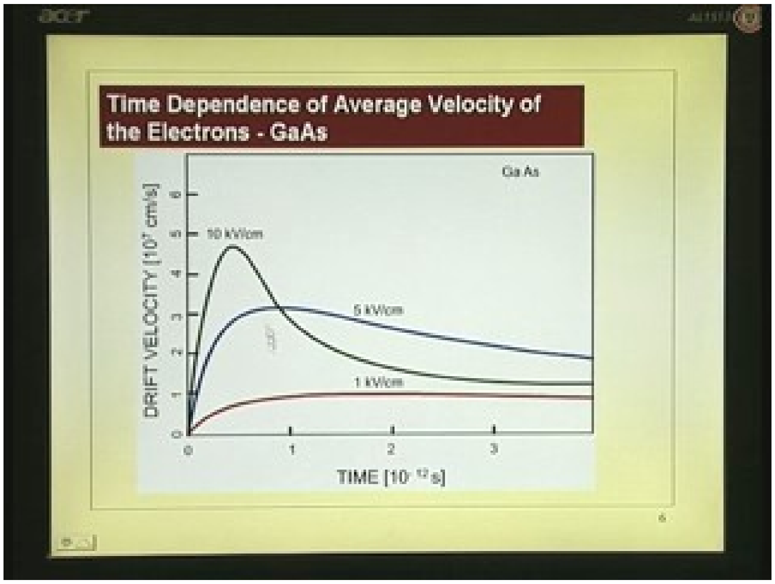

Time Dependence of Average Velocity of the Electrons - GaAs

What we saw last time was in addition to this, this is the steady state effect. In addition to this, we have the transient effect and that transient effect is like that. The transient effect, for example in gallium arsenide, it takes time for the velocity, for example, if you take 1kv per centimeter, that is go back to the curve and see.

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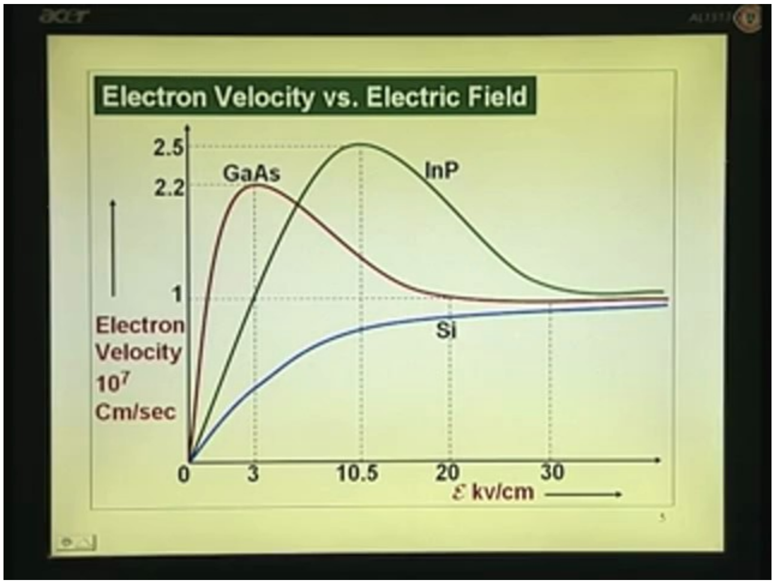
Electron Velocity vs. Electric Field

If you take 1kv per centimeter, in gallium arsenide it is some where here. For electric fields lower than 3kv per centimeter, electrons are all in the lower valley, they never get transferred to the upper valley. They do not go through this; they do not enjoy the benefit of going through that peak field. In the sense, we put it in personifying the electrons so they will just get accelerated to that (05:35) value and they remain there. If the electric field is subjected to electric field or is subject to electrons, suddenly to high electric field. For example, if you subject into 10kv per centimeter you can see that is about the saturation velocity that is more than 1 into 10 to the power 7 centimeter per second. If you take a look at the velocity field characteristics of gallium arsenide, if you subject the electrons suddenly to the 1kv per centimeter, they will saturate out into that with time, which is what you see here.

I will go back and forth in between these two slides (Refer Slide Time: 06:19), 1kv per centimeter energy is not sufficient for transferring the electrons from the lower valley to upper valley. They will just increase and after a pico second or two pico seconds, they will saturate corresponding to that velocity. If you subject it to 5kv per centimeter, you can go back to that curve and see 5kv per centimeter somewhere here. It is more than the energy is required to transfer the electrons from the lower valley to upper valley. But it takes finite time for electron to transfer from lower valley to upper valley.

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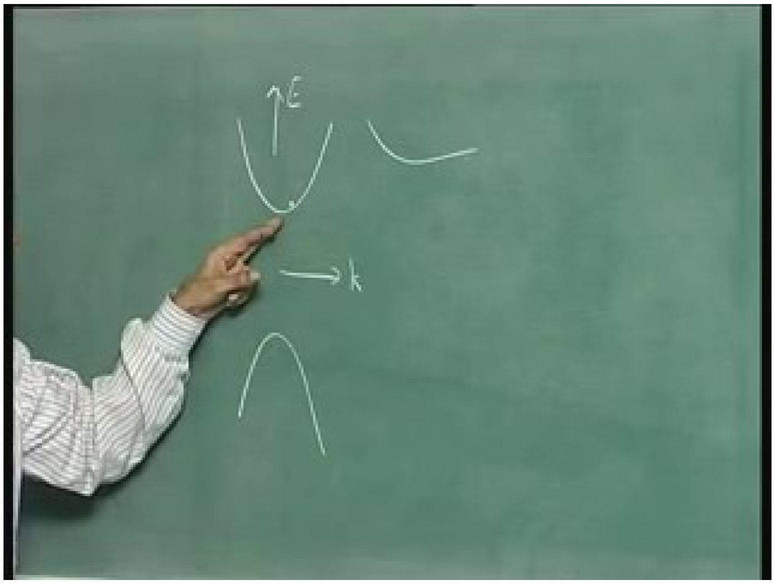

During that finite time, before it Trans scattered to the upper valley, it is all the time in the lower valley. As a result just keep that drawn here, what you have in that situation is, electrons are all the time here, during the transient time and if you subject them to high electric field, they accelerate much faster. So they even cross this energy and during the transient even if the networks is known, subject to sudden fall it gets overshoot effects will be there. Similarly, you get overshoot effect, because of that. That is why if you subject it to 5kv, it goes up, then ultimately if you wait long enough, it will saturate onto the velocity, since it is velocity governed by 5kv.

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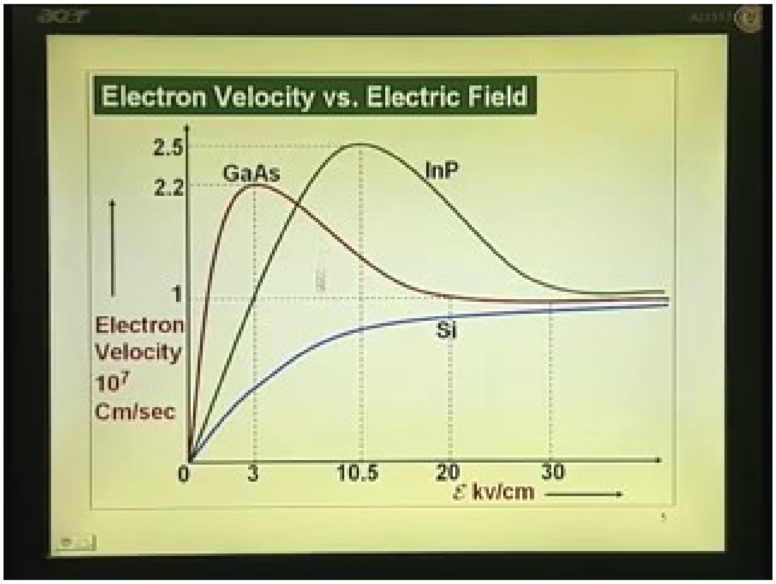
Electron Velocity vs. Electric Field

If you subject it to higher field suddenly, ultimately it will have to go into this velocity. You can just see that higher the field, the rate of change of velocity is very fast. It gets accelerated fast because of high field and it reaches even higher velocities and ultimately goes back to the saturation velocity. It goes quickly to its saturation velocity, because it retains that higher energy required quickly because it rises shortly. You see the peak here, when you apply 10kv per centimeter, occurs much before the peak that occurs here. It is because; it has gone to the higher energy very quickly. This is about the discussion, just summing up what I have discussed last time because some of the things I might have left out, so just thought of verifying some of them.

The same thing if we plot, actually the electron is getting accelerated with time, it also moves forward in space. In space also same behavior takes place, only instead of x axis being time, it is velocity into time that is distance.

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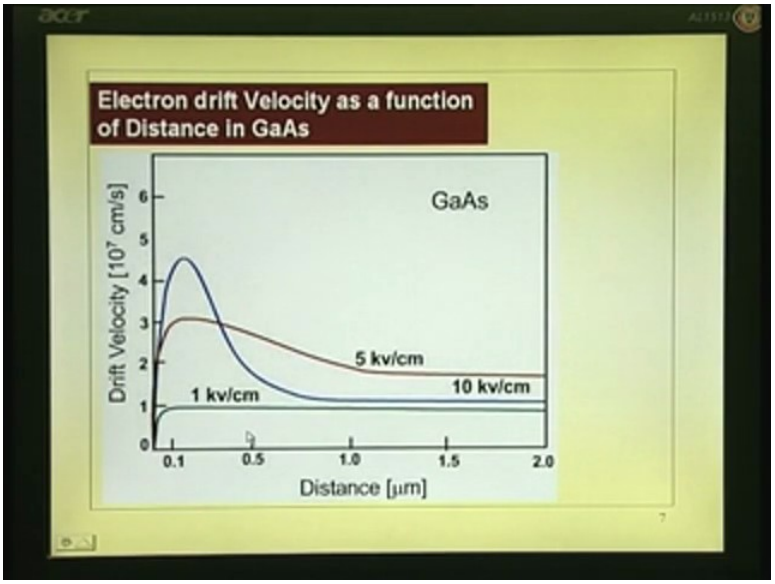

Electron drift Velocity as a function of Distance in GaAs

This gives us a better idea, because after all in the transistor, when you make a device what we see is how far would it move with that higher velocity? Thant is clear, for example, if you subject to 10kv per centimeter, then it have velocity in excess of 10 to the power 7 per centimeter; say 10 to the power 7 centimeter per second, over a distance up to about 0.5 microns. You can see now, if your channel length is less than 0.5 micron, it has not gone into that, the transient phase is not over, as a result through out the channel the velocity will be much higher than 10 to the power 7 centimeter per second. The time required for transient is very small, that is the transient time should be small because the average velocity is high and because of that you will get higher gm. These were the benefits if gallium arsenide is present.

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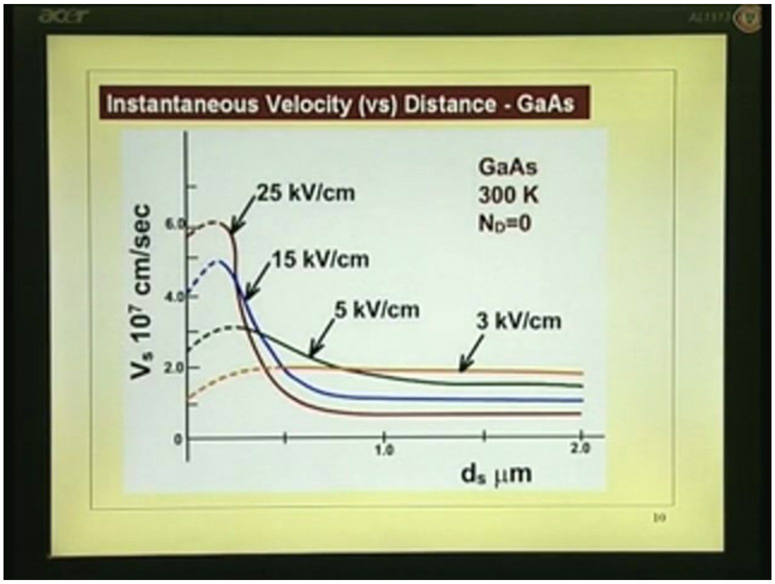

Instantaneous Velocity (vs) Distance - GaAs

Now let us take a look at indium phosphate. Let us go to indium phosphate first. Just before indium phosphate, I just plotted this for all different fields. For example, 3kv it saturates; if I go to 15kv it saturates in much lower value; 25kv it saturates at a saturation velocity. What you get here is a saturation velocity; what you get here is the velocity overshoot effect. You can see, about .05 micron channel length if you have, you will get very good benefit for case of gallium arsenide.

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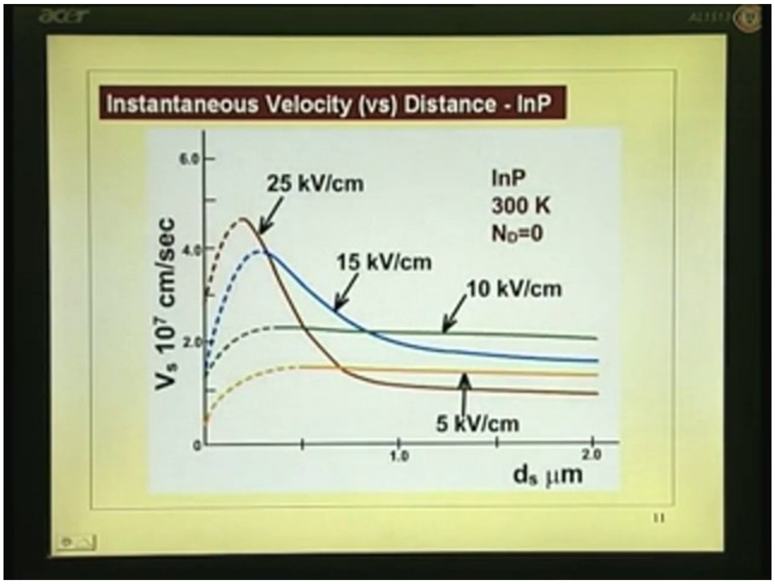

Instantaneous Velocity (vs) Distance - InP

Let us go to indium phosphate. Indium phosphate also similar transient, the difference is this gap (Refer Slide Time: 11:21) as pointed out is 0.53 electron volts. The electrons must have acquired much more energy. So the transient effect will be felt for longer time and it is felt for longer distance.

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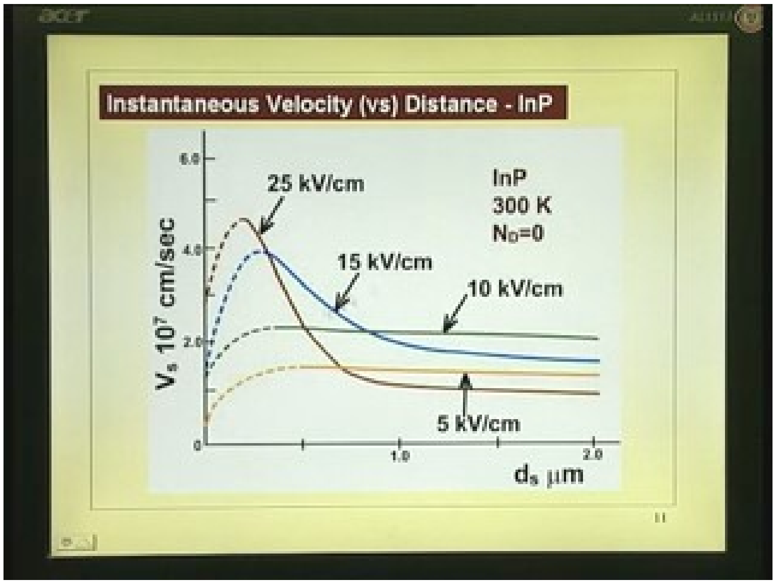

Instantaneous Velocity (vs) Distance - InP

Now, you can see here, supposing you subject electron suddenly to 25kv per centimeter. Almost up to 1 micron or at least 0.75 micron, the velocities are higher; whereas, if you take gallium arsenide, that velocity overshoot effect is over within our 0.5 microns; two gallium arsenide is over within our 0.7 micron. Because it gets transferred much easily compared to indium phosphate; indium phosphate takes more time because more energy is involved, it would get transferred to the upper valley. So, you get the velocity overshoot effect over a longer distance in the channel, in the sense you can get benefits in indium phosphate even with little longer channels, even if the field is quite high.

So, ultimately what we conclude is, if you take gallium arsenide and indium phosphate the mobility of electrons is high in the case of gallium arsenide; low field performance will be much better in the case of gallium arsenide, but when you go to high fields, you can expect the performance of indium phosphate to be better, but technology has developed much more with gallium arsenide. It is easier to handle gallium arsenide compared to indium phosphate. Because you move from silicon to gallium arsenide; gallium arsenide to indium phosphate, it becomes tougher and tougher to handle the wafer. In fact silicon is quite hard comparatively. Gallium arsenide, if you hold the Caesar, you can see it is more brittle and slightly softens. If you go to indium phosphate, if you press the Caesar and you can see the Caesar mark there and it is that bad. In fact I was fortunate enough to handle all the three types of wafer, you can feel and you have to be extra cautious if you want to do research in indium phosphate. This is the experience that you get with the small cut pieces but then the big wafers. You can see the guy who is holding the indium phosphate wafer will be shivering on his shoes, because that is double or three times costlier than that of gallium arsenide. That is why indium phosphate we used but very rarely, mostly people try to use gallium arsenide.

Now, here also you can see that if I use 10kv per centimeter, the field 10kv per centimeter, it is always lower value indium phosphate. Let us go back and see the steady state characteristics.

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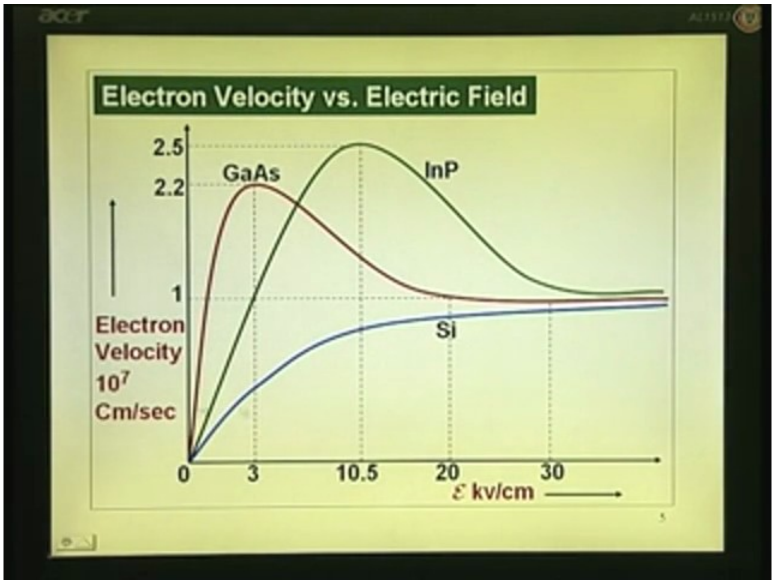

Electron Velocity vs. Electric Field

Just remember this, 10kv per centimeter that is peak. Till that peek is there we have analyzed and seen that the electrons are always in the lower valley, so if you apply field suddenly equal to 10kv per centimeter in the case of indium phosphate, it is never going to go in to upper valley. If you go on increasing and it will go to that. It does not experience that transient so much. That is why you see that particular effect there.

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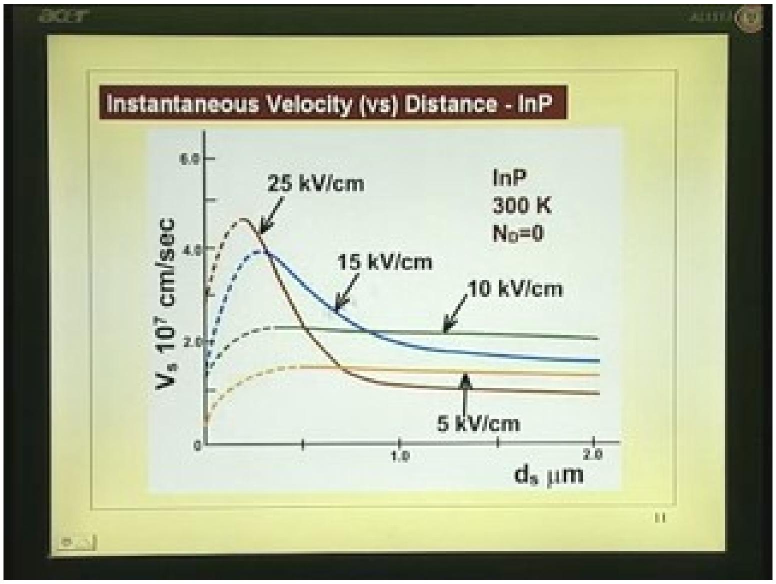

Instantaneous Velocity (vs) Distance - InP

One thing I just wording all the time is discussing the transient effect of silicon. When you say because of the difference in the momentum, as velocity increases, energy increases and the momentum also change. The electrons get transferred from the lower valley to upper valley, in the case of gallium arsenide and indium phosphate. As a result, you get this velocity overshoot effect because of that time difference between the relaxation times of energy and momentum. Momentum difference is so larger from one valley to other valley. So, silicon people started asking question, do you not see similar effect in silicon? Yes, we will see that. It will not be a transfer from lower valley to upper valley; it is the difference in the relaxation time between energy and momentum. It takes a different time for entire things to stabilize. So, because of that even in silicon, we will see some amount of transient that is what I projected here (Refer Slide Time: 16:08). But please note the time frames and also the distances. You do not have to deal this so much of difference in the momentum in silicon.

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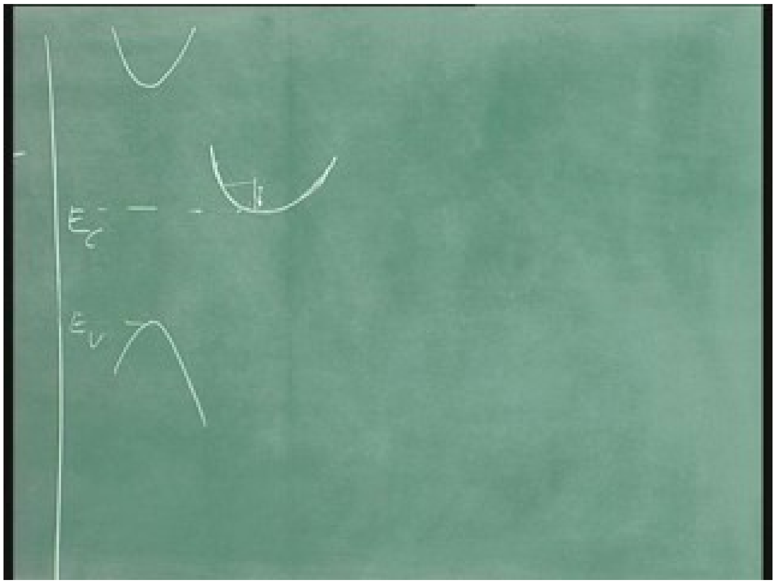

Here, (Refer Slide Time: 16:21) you have to deal with lot of momentum difference. You talk of silicon, then what you have is you may have large gap there and we have the small gap here. This is the conduction band edge; this is the valance band edge. Now, the electrons they do not get transferred on to that, everything happens within that, this gap is quite a bit.

Here, as the electrons acquire velocity, they also have to move into that position. Ultimately, this is the straight state curve. During the velocity energy acquire it will acquire energy in certain time, but it takes a time for that to relaxing to this steady state momentum. To put it in the language of physics, the relaxation time between the energy and momentum is slightly different, because of that you do see slight overshoot and coming back to that point. It may overshoot back and come back to the point because of the difference in relaxation times between energy and momentum. But the momentum difference is not so much as in the case of gallium arsenide etc., is not that much, it is only within that curve, EK diagram so that transient takes place within very short time.

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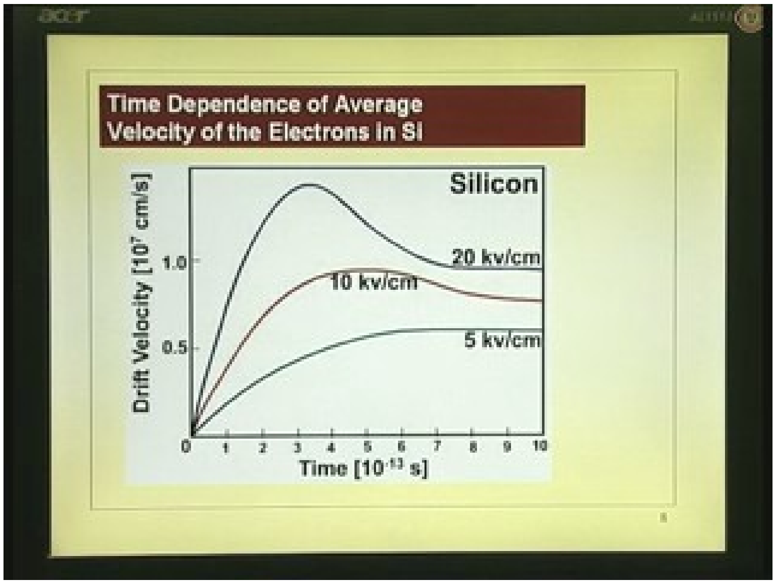

Time Dependence of Average Velocity of the Electrons in Si

You can see this dependence of average velocity of the electrons, these are simulated curves which we are projecting - 20kv per centimeter there is slight overshoot close to saturation, 5kv per centimeter it is much below the saturation velocity. Saturation velocity is 10 to the power 7 it occurs much beyond 20kv per centimeter or about 30kv per centimeter. If you subject electrons suddenly to 20kv per centimeter, you have that slight overshoot, but you see it is not much. It may be 1.25 into 10 to the power 7 as compared to three four times of 10 to the power 7 in gallium arsenide and indium phosphate. Plus, the entire transit effect is over in a very short distance. You could have hold silicon with this velocity overshoot effect, if these are retain for long time or longer path distance. If you multiply this velocity into time and find the distance over which velocity overshoot effect is present in the silicon that is the curve.

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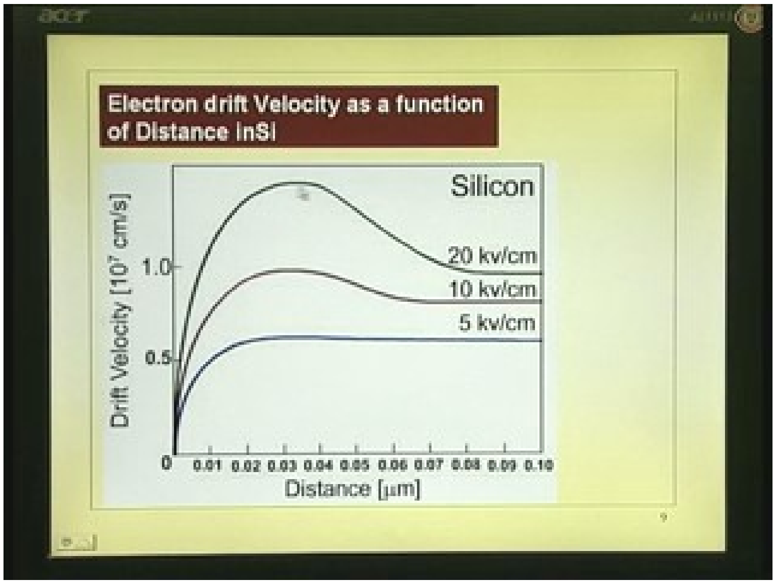

Electron drift Velocity as a function of Distance inSI

One thing that we have notice here is, these are 10 to the power minus 13, it is less than a pico second, entire thing about half pico second; whereas, in gallium arsenide it was pico second or more. Distances in gallium arsenide were 0.7 micro and indium phosphate 1 micron, after that you have got velocity overshoot effect. In silicon you can see, this is 0.07 micron, it is much less than 0.1 micron. If you want to get benefit of this velocity overshoot effect with silicon, what is the channel length that we should talk of? It is less than 0.1 micron.

When you head towards that channel length electrons will experience that, but even that experience is very marginal. It is not much to really be satisfied or really boost of for silicon, saying this has so much of velocity, this is just 1.25 of silicon or 1.75 that range, it is never 2. We have got less that 1.5, but you do get that so to be fair for silicon you get velocity overshoot effects but the benefit you will reap only if the channel lengths are very small of the order of 0.05 microns, which is very tough to achieve.

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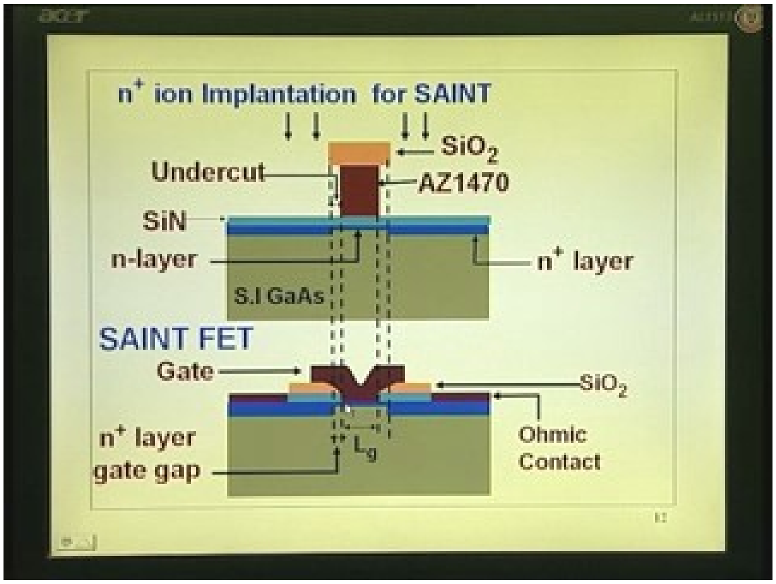

n^+ ion Implantation for SAINT

SAINT FET

Let us go back into what we have been discussing. Ultimately, we said if you have to have the velocity overshoot effects experienced, the electrons must be launched into the channel itself, which is short. If you are talking of a device like this, I do not go through the process again because we have gone through the whole thing. The key thing here is you must have the source n to the power plus and drain n to the power plus, you can see here. The final device structure is this. The ultimate device structure is we have got source n to the power plus, which is actually very close to the gate; this is the gate metal. The gap between the gate and source should be kept as small as possible. Ideally, they should be self aligned exactly, but you cannot do that, because there will be short circuit between the source gate and the drain. This is the gap; you call it as n to the power plus layer and the gate; gap between the n to the power plus layer and the gate.

The channel length is this, when apply voltage between the drain and the source that appears across this. Supposing it is 0.2 micron and you have applied 1 volt, it is 1 volt by 0.2 micron that is average field there. That is 10 to the power 5 by 2 that is 5 into 10 to the power 15kv per centimeter, it is large. You would definitely have velocity overshoot coming up. Keep this gap small, so that electrons are launched here and they reach the gate where the control is there immediately then, you get all the benefits right through. Supposing, the channel length is very long you do not get the benefit at all.

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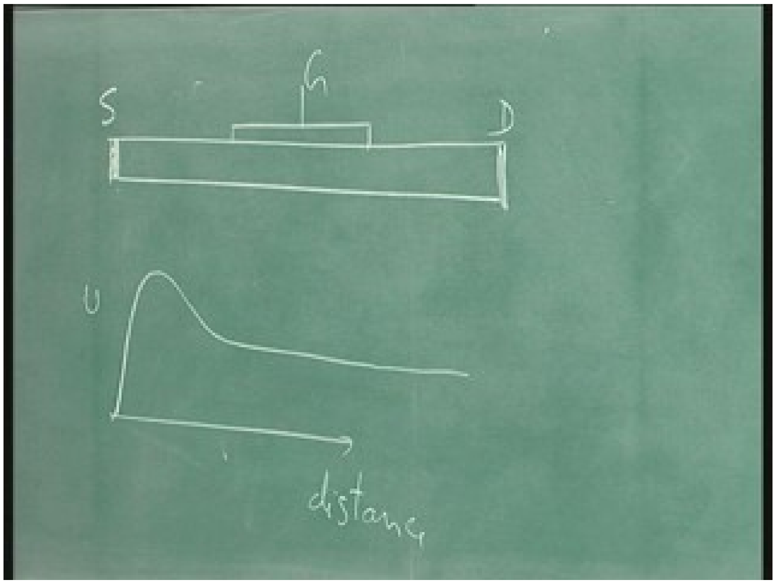

For instance, if I have a long channel with a gate; source, drain and gate. As the field is high, the electrons will actually acquire velocity verses distance. These electrons will go through. Most of the channel length the velocity is saturation velocity and they are subjected to 20kv or 30kvThat is the final velocity. This may be high but it is over before it reaches the gate; whereas, if this length is short this comes under that. The overshoot effect is seen under the gate itself. That is actually the real channel where you can control everything, current flow etc. You get the benefits if the channel length is shorter. You get the benefit of velocity overshoot effect; you will also get the benefit of high mobility when a field is low. That is as you vary the electric field, as you vary the drain voltage, electric field varies from low value to high value.

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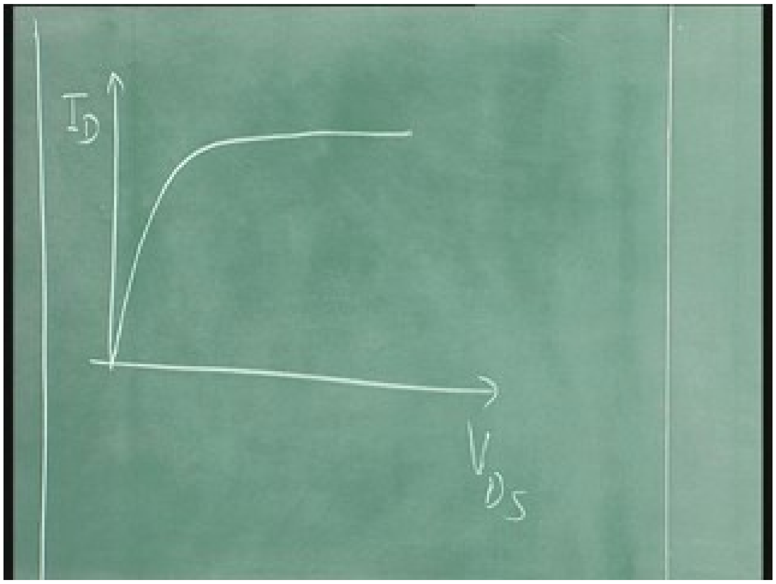

When electric field is low, let me just draw that here, side by side. Recall the V_{DS} versus I_D curve like that. This slope here, we determine by the low field mobility and this slope is actually on resistance of the device. You want this to be as steep as possible, from that point of view; you would like to use the device which has got high electron mobility. From that point of view, gallium arsenide scores over indium phosphate because of the high mobility. Gallium nitride, material that people are talking of is poor in that respect. Its mobility is not as high as gallium arsenide or indium phosphate around 2000. People are improving on a quality of the material to get better and better mobility in gallium nitride. Right now, gallium nitride is not for high speed devices; it is mainly used for high power devices because of high band gap, better thermal conductivity etc., similarly silicon carbide. This region you can control very easily or it is much better with gallium arsenide. You will see soon, how to get even steeper with high electron mobility transistors that we will see in a couple of lectures later.

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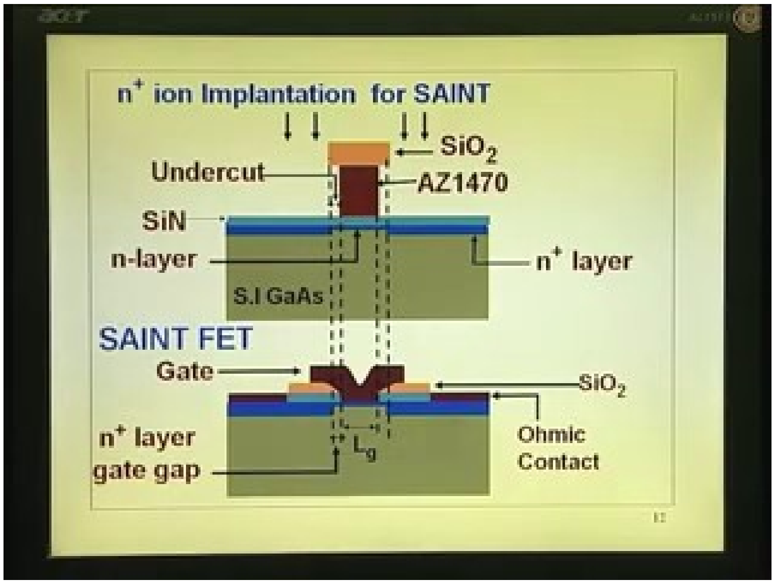

n^+ ion Implantation for SAINT

The key thing here is to have this layer closed. One thing it reduces the resistance that comes between this gate and the ohmic contact. The other thing is the velocity overshoot effects are felt very well. The technology involved is little complicated.

Let us take a look at how do these devices perform, if you have this implantation? Notice here, this region is obtained by a using this as a mask. What is the gap between this gate and this drain is decided by this undercut. That undercut is controlled by the etching time. You etch this layer from the top, as you start keep etching longer and longer the undercut is more. Even it is just 0.25 to 0.35 microns, very precisely I control the etching time, that all we discussed last time. Now, let us see what will be the effect of this gap between the gate and this n to the power plus layer. L_g is the not here. L_g is the gate length between the dotted line you have got the gap between the gate and the n to the power plus layer

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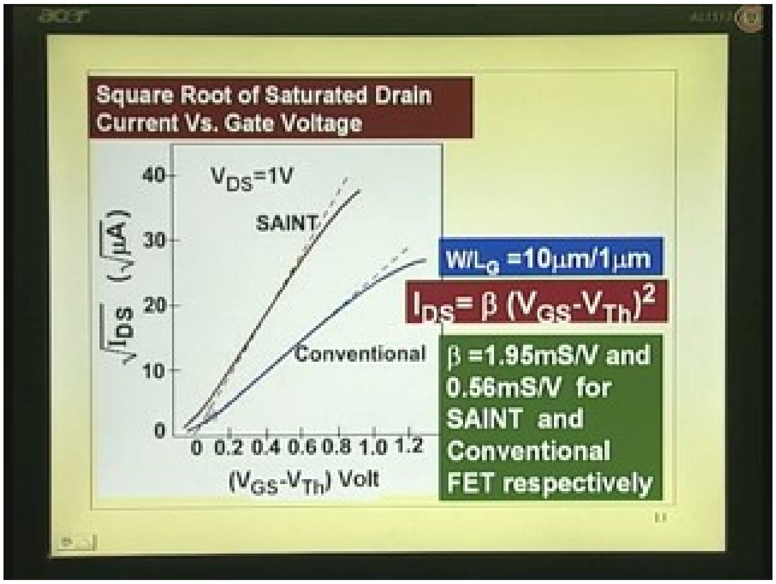

Square Root of Saturated Drain Current Vs. Gate Voltage

$W/L_G = 10\mu m/1\mu m$

$I_{DS} = \beta (V_{GS} - V_{Th})^2$

β =1.95mS/V and 0.56mS/V for SAINT and Conventional FET respectively

These are some of the results that people are reported way back, 20 years back. Some papers have appeared, when they have made these things, some of these devices, though the perfection came much later. Some of the preliminary results were reported there. What they are talking of is channel width is 10 microns that is the gate width, very small device. Gate length is 1 micron, 10 micron by 1 micron and you take for a V_{DS} equal to 1 volt, the root I_{DS} versus V_{GS} minus $V_{Threshold}$ voltage. If you plot, you get this sort of characteristics linear, root ID. Telling you square law, actually what we have showed even in the velocity saturation effects are there, it gives square law. There are two devices which are shown here: one is the SAINT and other one is conventional. The difference is only in the n to the power plus implant. Just go back once and see how it will be different.

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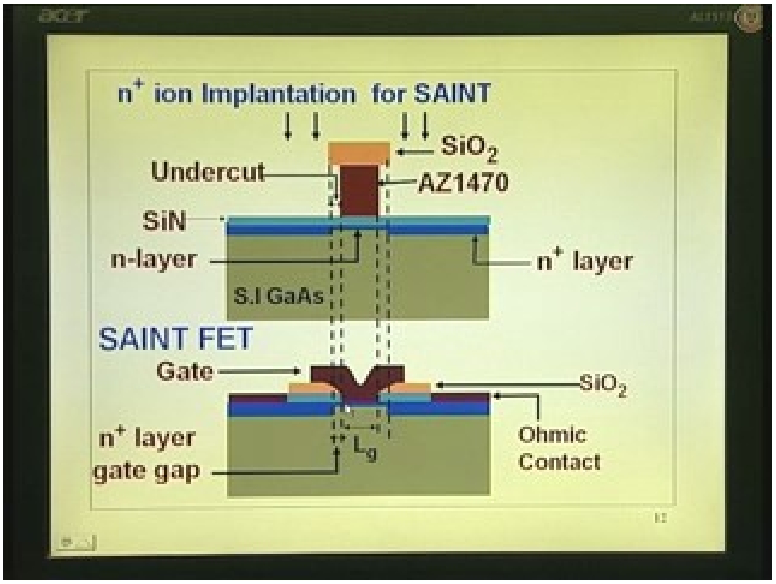

This is the SAINT, self aligned implantation technology for the transistor, n layer implantation technology. If you do not do that implantation, put the ohmic contact here and here same thing came, without n to the power plus layer, it is conventional. All process is becoming same, just avoid that n to the power plus layer, it is conventional. The difference is dramatic. See the two slopes (Refer Slide Time: 28:59) root I_{DS} versus V_{GS} minus $V_{Threshold}$. This is steep. We get much higher values of current for the same voltage and indicating you that factor beta are higher. In the case of SAINT, it is intact; this is 1.95 milli seamen per volts. Milli seamen are milliampere per volt, so 1.95 milliampere per volt per volt for SAINT. For this it is about 0.56 milli seamen. Ratio of about 3.4, ratio between this transconductance is 3.4, tremendous. The whole thing is due to two factors: one, this is actually the effective transconductance that you get, beta. One reason which everyone is familiar is the series resistance. If you do not have this n to the power plus layer you get the effect of the thin layers of the channel, which is dope larger lightly. The doping concentration in the channel is decided by other factors, the threshold voltage etc. So, you have the series resistance, the moment series resistance is there, the transconductance is lower, gm_0 by 1 plus gm_0 into rs. So, that pulls it down. Two, the velocity overshoot effect is present in this case in the channel itself, where if you do not have the n to the power plus layer that effect is not effective. These two things put together, we have got the better performance. This is the one thing I wanted point out.

Practically, it has been demonstrated and by factor of 3 to 4, in that range that is coming double. This is for one particular channel length and one particular gap width that they have provided about 0.3 or so micron.

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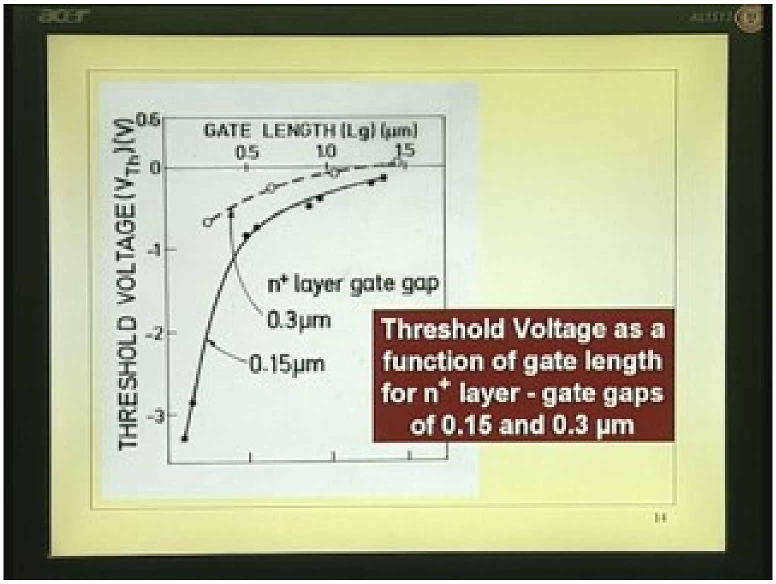

Threshold Voltage as a function of gate length for n^+ layer - gate gaps of 0.15 and 0.3 μm

Let us see the effect of that gap, the gap between the n to the power plus layer and the gate. Keep that focused, maybe I can go to this thing and show you (Refer Slide Time: 31:28). I would not be going back to this again and again, between this edge and this n to the power plus layer that is the gap, that we are talking off, which has the result of the undercut. What we are showing is the result that people have achieved with different gaps. What is the effect of that on the performance of the device? What are the parameters which you talk of performance? One is the threshold voltage and other of course is the transconductance that we have seen, it is already there, good effect. So this is the threshold voltage effect. On the x-axis you have got the gate length not channel length 0.5, 1, 1.5 and 0.25. You can go down write up to 0.25 micron channel length. Then if you measure the threshold voltage by root I_{DS} versus V_{GS} minus $V_{Threshold}$, you can plot and get the threshold voltage. That is the circuit engineer's practice to get the threshold voltage. When you do that, you get the threshold voltage more and more negative.

Go to shorter channel length, keeping the gap as 0.3 microns and keep the gate length keep on reducing. In other words, what is happening is I think better have the diagram here.

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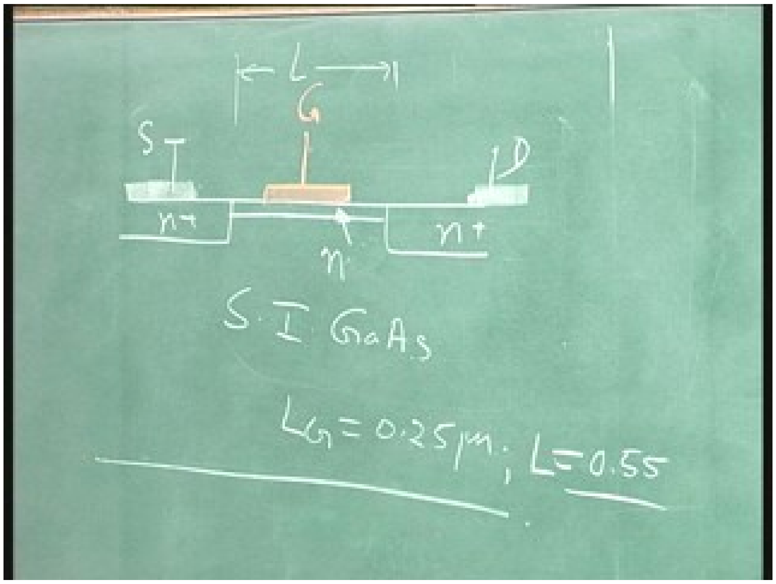

Now what we do is I can point this out better, let me have not complicated diagram. All that I am telling is n to the power plus layer here; n to the power plus layer there; of course the contact; the Source; the drain and we have got the n layer. That is the n layer. You have got the semi insulating gallium arsenide. The gate is here, that is the gate length L_g and this is the gap. What we do is, in one set of experiments, you keep this gap at 0.3 and reduce this gate length, which means when you reduce this and if you keep this gap same that is reduced. For a given drain to source voltage the fields are higher, notice this field is in this direction are higher.

If I reduce this distance and also cut this down, keeping the gap same because the voltage applied between the two the fields is high, the experiment that they have reported are: one case, this is kept at 0.3 microns, one curve and another curve where this is kept at 0.15 microns. In the case where this is 0.15microns, this gate length is 0.25 micron. This is 0.25 microns. 0.25 plus 0.15 and 0.15 that is 0.55 micron is the gap. When L_g is equal to 0.25 microns, you have this total length L equal to 0.25 plus 0.15. So, 0.3 plus 0.25

micron is equal to 0.55 micron that is what we get; whereas, is the other case, if this is 0.3, total length is 0.3 plus 0.3 is 0.6 microns plus 0.25 equal to 0.85 microns. You have got 0.85 microns in one case and another case 0.55 micron for the same channel length, gate length. The fields are much higher when the L is 0.15 micron

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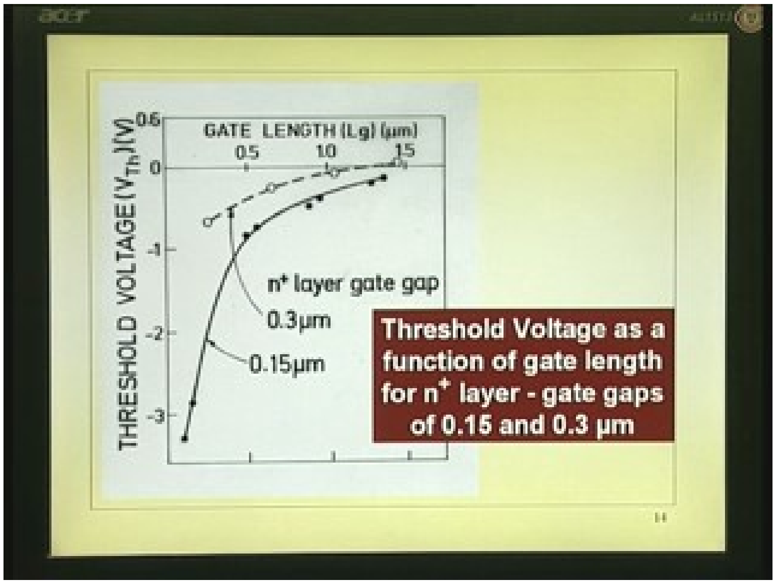

Threshold Voltage as a function of gate length for n^+ layer - gate gaps of 0.15 and 0.3 μm

Now in that back ground, just see this particular diagram, what is happening here? What we see is, when the channel length is long, for a 0.3 microns channel, for a 1.5 gate length, 1.5 plus 0.6, 0.3 on both sides. That is actually 2.1 micron. There you get threshold voltage of about 0, over slightly, close to 0. If you keep on reducing the gate length, in other words you are reducing the channel length itself; you get reduction in the electric field. The threshold voltage shifts negative. The effect is worse, if you keep the n to the power plus layer gap at 0.15, uncontrollable. See the threshold voltage is what is close to 0 here? When you reduce this something like 0.25, it is way down there, minus 3 volts etc, which you cannot tolerate. What could be the reason for this?

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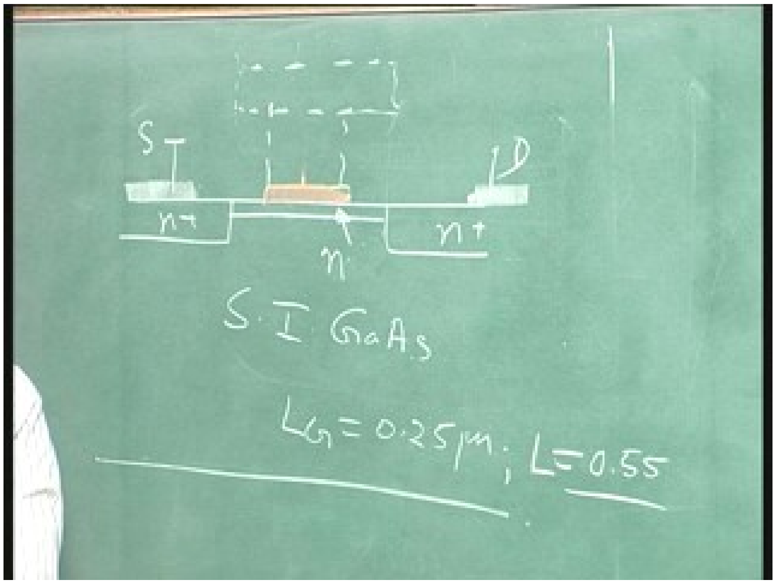

There are several reasons. One of the reasons is, if you remember this layer was implanted through the mask in a top. The layer was implanted like this. There was something on the top and I am just projecting this, because it was there when you implanted. That is why I am putting dotted lines. Layer was implanted using a mask. This under cut is 0.3 microns that is located away from this point. If it is 0.15 micron, that is closer. When you bring this closer and closer, one important thing that happens is it is not as if this implanted atoms they go just rest vertically. This is the statistical phenomena. When implanted, where it goes and lands. When you implant like this here, the atoms just come here, ions come there, they get utilized of course when land in the atom, because the electrons come from the back door, from other contact. So when it lands it is neutral after it is landed. You have the dream current which decides how many atoms are coming

The atom can rest here or here or there, that is called straggle statistical phenomena. In the sense, if you take the doping profile here it goes through a peak and the peak corresponding to what is known as a projected range. Most of the atoms land there. Similarly, the atom not only has got right to move in the direction anywhere like that, it can also go like that. It goes here or there, when it comes, it hits the host atom and like a billiard's ball hits it, deflects it and it also moves. So, both the host and the guest suffer the impact of the things. The energy transferred is proportional to the masses; heavier the masses, a heavy fellow colloids you, you can talk more; the lattice atom gets lot more. So the energy transferred is more. They rest earlier. Anyway what I am trying to point out is, it colloids with one of the motions of the implanted atom, collision and deflection will take place till the entire energy is lost. That is the philosophy or theory behind the ion implantation. Where it lands? (Refer Slide Time: 40:34) When it moves here or here or there or there depends upon the angle with each they are centered. After all we are talking at atomic level. When it comes and hits it. If I have two atoms, one atom is lying here, other one coming and hitting directly then, the weight scatter is different. If it comes at an angle, it will scatter in different way. You have struggle in this direction and also in this direction. That will be at least one third or one fifth of the distance which moves it can be distributed.

You will have a peak distribution, like this (Refer Slide Time: 41:17). When hundreds of atoms come they can be distributed like this, it can be distributed like that also. What I am trying to point out is, an atom which comes up here (Refer Slide Time: 41:27), we have drawn it is nicely on the board, saying that this is where the n to the power plus layer is, but actually comes and enters into the channel. It enters here.

How much it enter? It will enter even in the channel, closer and closer to reduce the gap. It will enter into a channel also. If it enters both this side and this side; if it enters into the channel, what is the result? The dopants are more, threshold voltage become more and more negative. Average dopants concentration becomes more because of lateral straggle. Because of the atoms which are implanted very close to the channel, getting into the channel. That is one of the main reasons, why the threshold voltage becomes more negative. As a result, the advice that people give is do not bring it that close, use SAINT, it will no longer be a SAINT, it will give trouble, if you place it too close. This gap is generally recommended about 0.3 microns is ok; for those energies above 0.3 microns is alright; less than that you will have threshold voltage shift, when you want to have shorter channel lengths. That is the sort of effect you have, that is one thing. Now you can explain the shift negatively. You can explain by this, because between this curve and this curve (Refer Slide Time: 43:13), the only difference is gap. But why should it shoot up here so much? When we go to very short current and shorter gate lengths, this way move parallel to almost, but shooting up like this beyond that point up to this point is ok, but beyond that point it is too large a change. You have to get in to the little bit of physics of this

The physics of this is, the field in this direction, see, we are talking of the voltages which are actually 1 volt or 2 volts here, but 1 volt divide by 1 micron and 1 volt divided by 0.55 micron, high field. You have got fields in this direction, which is high. Now let us see what happens? Infact the threshold voltage measured by using that I_{DS} versus V_{GS} at one particular field, voltage. Let us see what happens.

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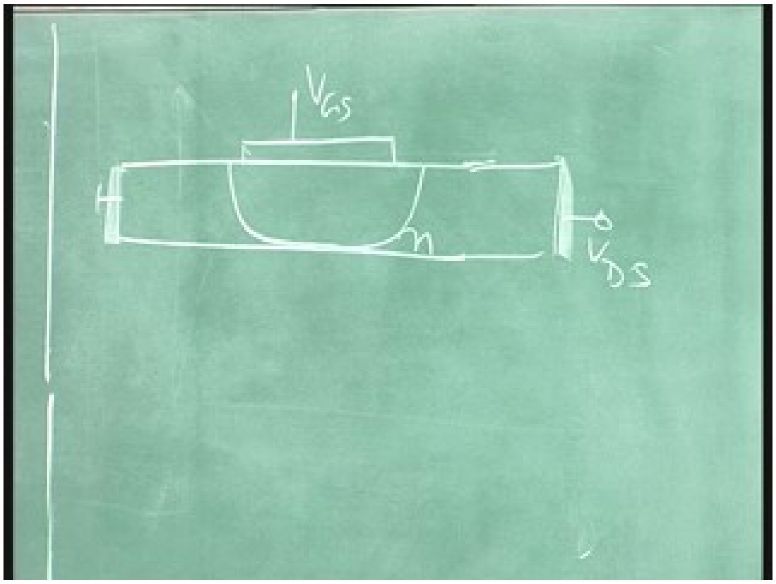

Let me just draw this diagram with amplifier. Suppose I have a channel like this and that is n layer. I am just magnifying that. I have the contact far away, corresponding to that that is the contact. Physically it is not ohmic; not the metal, but electrically that is the contact. When I apply voltage between these two, and this is V_{DS}. I am showing on this is n layer. What is threshold voltage? Threshold voltage is voltage that is applied to the gate to close the channel at the source end. If this voltage V_{DS} is not there, we saw reducing this, the effect of pinch of voltage and threshold voltage. That is one effect that is seen here and you will get a thing like this. That way you get. Reduce the channel length, gate length, you get these two merging together, the pinch of voltage changes, threshold voltage becomes negative that also we saw. Threshold becomes more, the pinch off voltage becomes more, as the result we have got more and more threshold voltage and that is seen. That effect should have been same in the case when it is 0.15 micron or 0.3 micron, the curvature effects, but something more happens. The way you measure threshold voltage, you are seeing the threshold voltage the V_{DS} applied that is not important for you. When applied V_{DS}, when we can shut of this device

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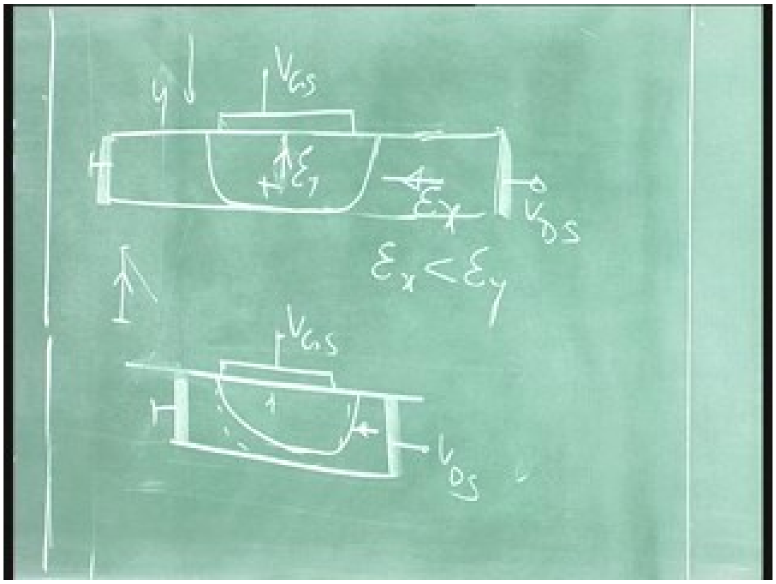

So, what happens is, this is like this. Provided all the field lengths are vertical or even cylindrical. Whatever it is, it is coming like that. But when I have the field like this, which is not anymore negligible. If that is larger what happens? How will the depletion layer be? This is very interesting thing; in fact one can stimulate and see when 2D effects are there. Let us put a different diagram. This is E_x. E_x less than E_y, Y in this direction that is E_y. In this case it will actually be like this because plus charges here and minus charge there and channel is depleted. Now, E_x is comparable to E_y, it will not just go down like that, even when the channel length is long. It will go like this, if this gap is reduced, if we keep it changed for the same gap, I bring it down here. I must reduce this. In the same device, all that you did is put the contact here and V_{DS} here. Now, what will happen will be let me just draw it a bit less. What will happen is, because this field is large compare to this particular field the depletion layer will not just come down vertically, even if it is one dimensional, even if it is cylindrical, it will not come like that. The whole thing will get dragged on to the other side. So what happen will be I am going through the whole thing qualitative way because there is no other choice for me other than you get some other result. So this will actually go down, this is like this. So instead of being like this, it becomes shifted like this. It does not close here. Idea is like this, I have one field line like this then I will have certain depletion layer width, but if the field line is dragged like this; the depletion layer width will be smaller. Instead of coming all the way down, because the field lengths are pushed in that direction because of the combined effect of the two, you get whole thing dragged like that. Result is the depletion layer width takes more voltage to close the depletion layer width. You must have higher fields in this direction, so that it is able to close.

One of the electric field is pushing it down like this, other one is pushing it different direction, the two dimensional. So as a result, you require larger field in this direction to close the channel. That is why, when the field in x direction is larger, in situation where the field in x direction is larger you require larger field in the vertical direction, that means larger voltage is closed down, that means larger is the threshold voltage, negative. If the field is larger, this voltage is larger negatively in that direction. What is the difference between the two cases? Here the channel length is long, for a given voltage there is certain field in this direction. Here the channel length is small, for same gate length. Channel length is long, so fields are larger here and two dimensional effects much more here compared to that. The entire depletion layer gets dragged on in one direction. So, it takes more voltage here to close down the channel that means threshold voltage is larger, negatively. The difference is gap here is more, gap here is less. The gap is less; fields are more along the channel.

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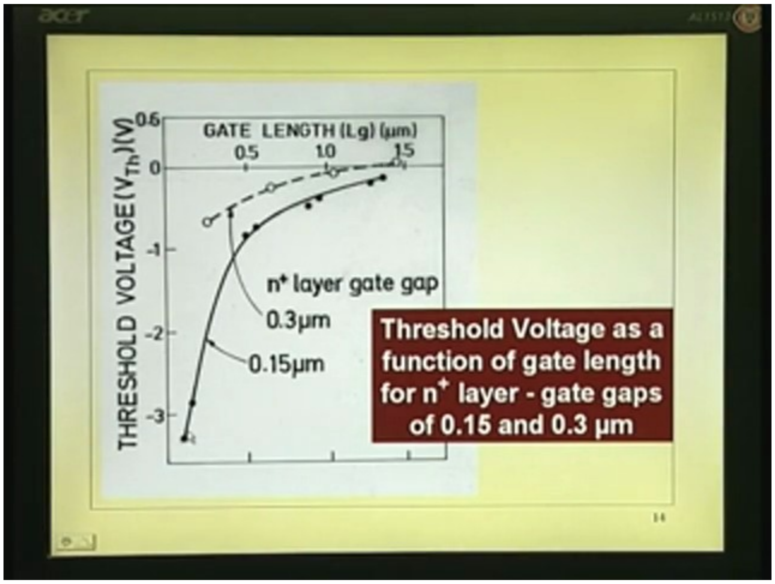

Threshold Voltage as a function of gate length for n^+ layer - gate gaps of 0.15 and 0.3 μm

So, you can see the impact of that you see more and more as you go into shorter and shorter gate lengths. Because when you go down here, the gate length and gap becomes more and more comparable. Channel length is shorter and shorter, you get the two dimensional effects much more here. When short channel devices there are two things one has to worry about. One is the curvature effect itself increases the threshold voltage. Second one is the two dimensional effect of the electric field also increases the threshold voltage. What is the way you can overcome this? I want to reduce the channel length, because I want to get a velocity overshoot effect etc., better and better. But you land up in problem because you have this two dimensional effect coming up. How do you cut down that?

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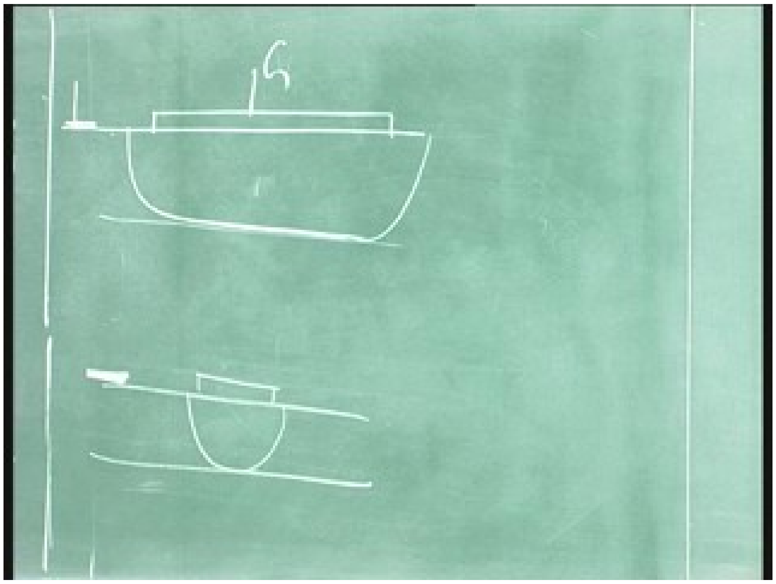

The answer is what you have discussed already. We said if I have a long channel, even if the drain voltage is not applied you will get it like this, the depletion layer. If you make the channel short, you have seen that for same thickness, it will be like that. This threshold voltage is larger than that that you have seen. How do we avoid that problem? Make the thickness smaller, so that depletion layer width is small compare to that. This curvature, you have a plain parallel portion there, you reduce the channel thickness and it must be accompanied by increasing in doping

The two dimensional effect, how do you reduce? This you are able to do because you reduce it so that there is a flat portion. Flat portion decides your threshold voltage but in the thing that we are discussing, only way for you is to ensure that the field in vertical direction is still large compare to field in the… See the whole thing shifts in the depletion layer towards the drain, distortion in the electric field and the depletion layer edge has come about because of that field becoming comparable to the vertical field. If you want to reduce that lateral field, you cannot do that. If you reduce the channel, it becomes higher and higher, but make that small compared to this vertical field. How do you do that? Increase the vertical field. How can you increase the vertical field? Reduce the thickness and increase the doping, vertical field is more. For given thickness, the doping is more, you have got automatically increase in the vertical field. So that way it is just like saying I want to reduce the length of one line, you draw longer line near that. Increase the field in vertical direction by increasing the doping.

Completely what we are trying now is you can have the benefit of better performance by increasing the doping in the channel. Increase the doping in the channel and also reduce the thickness, you cannot keep on reducing the thickness but you can increase the doping. You can increase doping up to five times 10 to the power 17 but you cannot go beyond that. What happens if I go beyond that doping ten times or five times of 10 to the power 17 or 10 to the power 18, maximum and minimum, this will become ohmic. It will no longer be acting as a rectifying contact. There is an upper limit to doping concentration that you can go. More than that, if you go to higher and higher doping concentrations, there is one parameter for which recommended gallium arsenide that detoriates.

What is that parameter? Mobility, mobility keeps on falling. So, the on state effect gets affected and also the velocity overshoot effect that you get, that effect also goes down. Because related which raises it is the mobility if the doping is increased, the slope reduces, so the velocity field characteristics goes bit slower. As a result, you do not get the velocity overshoot effect as much as you want. From this point of view, you will have to look into other type of devices, where you can still have doping; doping region, separated from the region where the electrons are present. That we will see may be one lecture after this that is high electron mobility transistors. I have few things to discuss, which I will continue in my next lecture. That is things like the sub threshold slope. I have to discuss what sub threshold slope? How that effects? Why you should worry about that? I will discuss in next lecture and then we will go to high electron mobility transistor.